Proceedings of the 15th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2008, August 31 - September 3, 2008, Malta, pp. 17-20.

A Pseudo-Differential Transmitting Circuit Causing Reduced Common-Mode Current Variations

Frédéric Broydé and Evelyne Clavelier
Excem
Maule, France
fredbroyde@eurexcem.com

***Abstract* — This paper introduces a new type of pseudo-differential transmitting circuit (TX circuit) such that signaling ideally produces no common-mode current variations in the terminals intended to be connected to the interconnection. These terminals are expected to behave as if the TX circuit was composed of a floating circuit and a two-terminal circuit element connected between the common terminal and ground. This is in contrast with conventional pseudo-differential TX circuits in which the generation of signals produces a variable return current flowing in the reference conductor. We present a detailed design and provide simulation results. We then consider the implementation of this TX circuit in a pseudo-differential link. This link is capable of low reflections and a reduced common-mode current. It consequently offers a good protection against external crosstalk.**

I. Introduction

In this paper, we consider a transmitting circuit (TX circuit) intended to be used in a pseudo-differential link (PDL) providing m channels, m being an integer greater than or equal to 2. Each channel may be used for transmitting analog or digital signals, from a source to a user. A PDL providing m channels [1, § 4.2.3] uses a multiconductor interconnection having m transmission conductors and a common conductor distinct from the reference conductor (ground). A PDL having $m = 4$ transmission conductors (numbered from 1 to 4) is shown in Fig. 1. The TX circuit receives at its input the signals of the 4 channels of the source, and has $m + 1 = 5$ output terminals: one signal terminal (ST1 to ST4 in Fig. 1) connected to each one of the transmission conductors and one common terminal (CT) connected to the common conductor. The receiving circuit (RX circuit) has its 5 input terminals connected to the conductors of the interconnection, and its output terminals connected to the user.

Many conventional PDLs do not use any termination [1] [2] [3]. Since some do, a termination circuit has been included in Fig. 1, but it may or may not be present. When a termination circuit is present, it is typically made of grounded resistors [4] or of resistors connected to a power supply voltage, e.g. when integrated circuits of the Gunning Transceiver Logic (GTL) family [5] [6, pp. 2-3 to 2-17] are used.

In a conventional PDL, the RX circuit ideally responds only to the m voltages between one of the transmission conductor and the common conductor. The routing and geometrical shape of all conductors of the interconnection being matched, it is expected that nearby circuits will induce practically equal disturbance voltages between each conductor and ground, so that noise cancellation occurs in the RX circuit. Thus, pseudo-differential signaling is intended to provide a protection against external crosstalk, using fewer terminals in the TX circuit and RX circuit than differential signaling (*external crosstalk* refers to crosstalk between the PDL and other circuits, whereas *internal crosstalk* refers to crosstalk between the channels of the PDL).

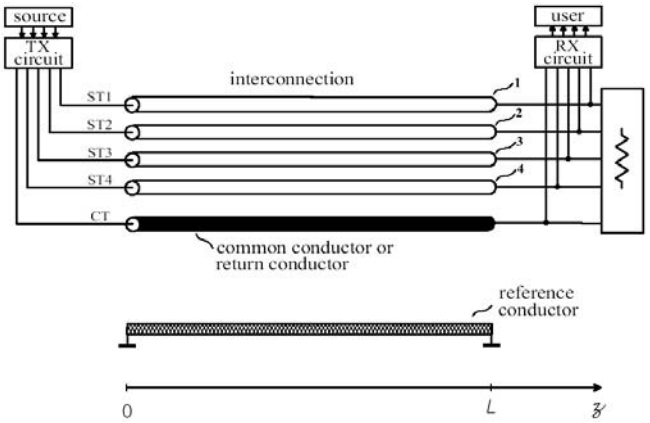

Fig. 1. A pseudo-differential link (PDL). The block containing the resistor symbol is a termination circuit which may or may not be present. The designation "common conductor" applies to conventional PDLs while "return conductor" applies to the PDLs considered in Sections II and IV.

Section II presents the specifications of a new type of TX circuit for pseudo-differential transmission. Section III shows the performances of a TX circuit meeting these requirements. Section IV presents simulation results for a PDL using this TX circuit and an interconnection comprising a wide return conductor.

II. Specification of a New Type of TX Circuit

The new type of TX circuit defined below and the MIMO series-series feedback amplifier (MIMO-SSFA) [7] recently introduced by the authors are quite different, but they share the characteristic of being inherently multiple-input and multiple-output interface circuits.

The new TX circuits are intended to be used with an interconnection having a structure such that it can be approximately modeled, for the propagation of signals in the PDL, as a $(m+1)$-conductor multiconductor transmission line (MTL) [8]. This implies that the propagation of electromagnetic fields mainly occurs within the interconnection and that the reference conductor is not significantly involved in the propagation of signals, provided the PDL uses the common conductor as a return path for the currents corresponding to the signals sent in the transmission conductors.

The designation "return conductor" appears in Fig. 1. It will be used hereafter, because it should be preferred to "common conductor" when this conductor may be, and is, used as a return path for the currents corresponding to the signals. This result can be obtained when the shape of the return conductor is such that it in a way shields the transmission conductor from ground [8]. For instance, interconnections having the cross-sections shown in Fig. 2 are appropriate to obtain this result.

For any integer j such that $1 \le j \le m$, let us use i_j to denote the current

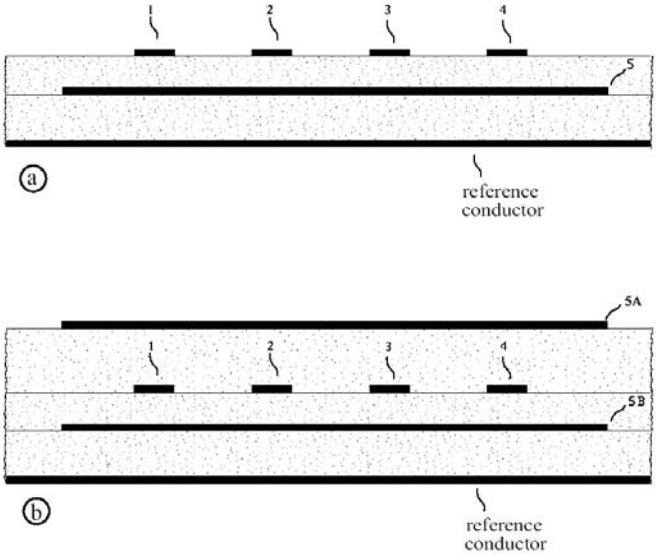

Fig. 2. Two possible cross-sections for the interconnection used in the ZXnoise method, where 1 to 4 are the transmission conductors, where 5 is the return conductor in the coplanar-strips-over-return-conductor structure (*a*) and where the return conductor is made of 5A and 5B in the coplanar-strips-inside-return-conductor structure (*b*).

flowing out of the signal terminal number j (STj). Let us use i_C to denote the current flowing out of the common terminal (CT). Using the return conductor as a return path for the currents corresponding to the signals implies that the TX circuit does not cause any variation of the common-mode current $i_1 + ... + i_m + i_C$.

In order to be compatible with this condition, the TX circuit must, for the interconnection, approximately behave as if the TX circuit was composed of a floating circuit and a two-terminal circuit element connected between the common terminal and ground, the floating circuit having exactly $m + 1$ terminals connected to the m signal terminals and to the common terminal. The corresponding equivalent circuit is shown in Fig. 3, for $m = 4$, in the special case where the two-terminal circuit element is composed of an impedor (i.e. a passive linear two-terminal circuit element) of admittance Y_D and a current source delivering a current i_{C0}. Since this current source is the only cause, within the TX circuit, of a possible common-mode current, i_{C0} must be a constant current.

The case $Y_D = \infty$ corresponds to a TX circuit using ground as common terminal. In this case, the TX circuit is a standard line driver. An ideal new TX circuit corresponds to the equivalent circuit of Fig. 3, in the case where Y_D is finite. In practice, Y_D might range between 1 mS and 1 S. Such values may be appropriate for

— avoiding that currents caused by nearby circuits, which normally flow in the reference conductor, use the return conductor as an alternate path; and/or
— damping the resonances of the common-mode currents caused by unwanted couplings.

Let us use v_C to denote the voltage between the common terminal and ground. According to Fig. 3, we want that, when the TX circuit is in the activated state, at a given frequency $f \neq 0$

$$i_C \approx -\sum_{\alpha=1}^{m} i_\alpha - Y_D v_C \tag{1}$$

The TX circuit is ideal if, in the activated state,

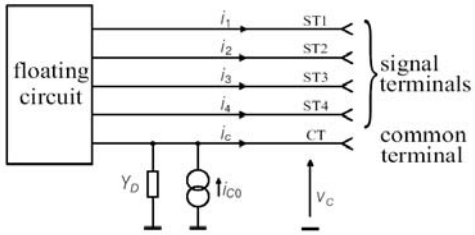

Fig. 3. Ideal circuit seen by the interconnection looking into the TX circuit.

$$i_C = -\sum_{\alpha=1}^{m} i_\alpha - Y_D v_C \tag{2}$$

If we now consider a non-necessarily ideal but linear TX circuit in the activated state, it is characterized, for the interconnection, at a given frequency $f \neq 0$, by

$$\begin{pmatrix} i_1 \\ \vdots \\ i_m \\ i_C \end{pmatrix} = -\mathbf{Y} \begin{pmatrix} v_1 \\ \vdots \\ v_m \\ v_C \end{pmatrix} + \begin{pmatrix} i_{1SC} \\ \vdots \\ i_{mSC} \\ i_{CSC} \end{pmatrix} \tag{3}$$

where $\mathbf{Y}$ is an admittance matrix and where the currents $i_{1\,SC}$, ..., $i_{m\,SC}$, $i_{C\,SC}$ are linearly determined by the m input signals. Consequently, we may consider that v_1, ..., v_m, v_C and $i_{1\,SC}$, ..., $i_{m\,SC}$ are arbitrary, but not $i_{C\,SC}$. We are looking for the condition corresponding to an ideal linear interfacing device. If we use the first m rows of (3) in (2), we get

$$i_C = \sum_{\beta=1}^{m} \left(\sum_{\alpha=1}^{m} Y_{\alpha\beta} \right) v_\beta + \left(\sum_{\alpha=1}^{m} Y_{\alpha m+1} - Y_D \right) v_C - \sum_{\alpha=1}^{m} i_{\alpha SC} \tag{4}$$

while the last row of (3) may be written

$$i_C = -\sum_{\beta=1}^{m} Y_{m+1\beta} v_\beta - Y_{m+1m+1} v_C + i_{CSC} \tag{5}$$

A comparison of (4) and (5) leads us to the following conclusion: the linear interfacing device is ideal if and only if

$$\begin{cases} \forall \beta \in \{1, \ldots, m\} & \sum_{\alpha=1}^{m+1} Y_{\alpha\beta} = 0 \\ Y_D = \sum_{\alpha=1}^{m+1} Y_{\alpha m+1} & \\ i_{CSC} = -\sum_{\alpha=1}^{m} i_{\alpha SC} & \end{cases} \tag{6}$$

Consequently, the TX circuit should comprise a balancing circuit capable of delivering the current $i_{C\,SC}$ determined by the input signals, complying with the last equation of (6).

If we want to measure the parameter Y_D of an ideal linear interfacing device, (3) and the first 2 equations of (6) imply that any voltages or currents may be applied to the signal terminals and the common terminal, as long as the voltage between the common terminal and ground is measured and the common mode current $i_1 + ... + i_m + i_C$ is determined. This is in fact visible in Fig. 3.

If the TX circuit is not assumed to be ideal, Y_D is clearly not uniquely defined by (1) alone. Consequently, in this case, the value measured for Y_D depends on the voltages or currents applied to the signal terminals. However, for a given configuration, we will define Y_D as the ratio of the

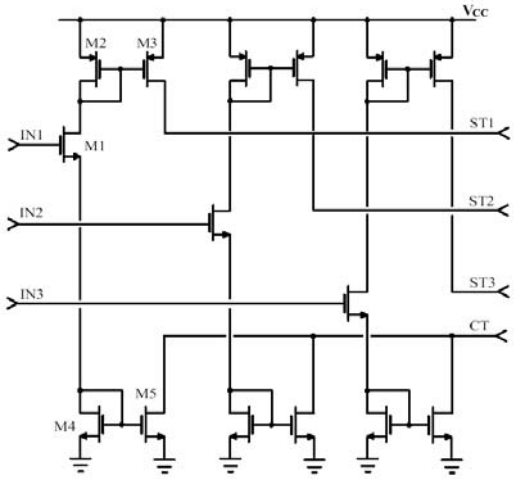

Fig. 4. A pseudo-differential TX circuit, for $m = 3$ channels.

common-mode current to a voltage applied between the common terminal and ground *in this configuration*.

Y_D being now uniquely defined in a given configuration, the error at the output of the balancing circuit in this configuration may be defined, at a given frequency $f \neq 0$, as

$$\Delta i_C = i_C + \sum_{\alpha=1}^{m} i_\alpha + Y_D v_C \quad , \tag{7}$$

this error being zero when the TX circuit is ideal. Consequently, we may consider that the common-mode current $i_1 + ... + i_m + i_C$ contains a legitimate part $-Y_D v_C$ and an illegitimate part Δi_C.

III. A Pseudo-Differential TX Circuit

A TX circuit producing reduced common-mode current variations is made, for each channel, of a single transistor phase splitter driving the inputs of two current mirrors of opposite polarity. The resulting circuit for $m = 3$ channels is shown in Fig. 4. When the inputs (IN1, IN2 and IN3) are grounded, the TX circuit is in the deactivated state (i.e. the output terminals present a high impedance). When the inputs provide the signals and a suitable biasing, the signal terminals (ST1, ST2 and ST3) source the output currents i_1, i_2 and i_3. The common terminal (CT) would sink $-i_C = i_1 + i_2 + i_3$ in an ideal implementation. In this activated state, the NMOS current mirrors (M4-M5, etc) clearly form a balancing circuit complying with the third equation of (6). At low frequencies, the error at the output of the balancing circuit can only be caused by non-ideal current mirrors. We note that the output admittance of the PMOS current mirrors (M2-M3, etc) is by itself a departure from the ideal equivalent circuit of Fig. 3, unlike the output admittance of the NMOS current mirror which merely contributes to Y_D.

We have simulated a 4-channel version of this circuit in a configuration in which the signal outputs ST1 to ST4 and the common terminal CT are connected to the test circuit shown in Fig. 5, the current i_C being measured at the point shown in Fig. 5 (consequently, the damping resistor Rc and the biasing voltage source Vco are now regarded as a part of the TX circuit). We have used the standard transistors of a 0.5-µm CMOS process for which the propagation delay of two-transistor CMOS push-pull inverters is about 100 ps in a ring oscillator. We used $W/L = 100/0.6$ for the input transistors (M1, etc) and $W/L = 200/0.6$ for all other transistors. For a biasing such that all MOSFETs operate in the saturation regime (V_{CO} of Fig. 5 is 3/10 of the power supply voltage V_{CC}), we obtain the small-signal frequency

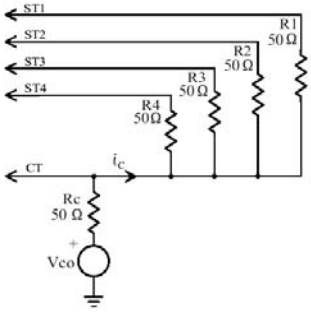

Fig. 5. Test circuit used for the assessment of the 4-channel TX circuits discussed in Section III and in Section IV.

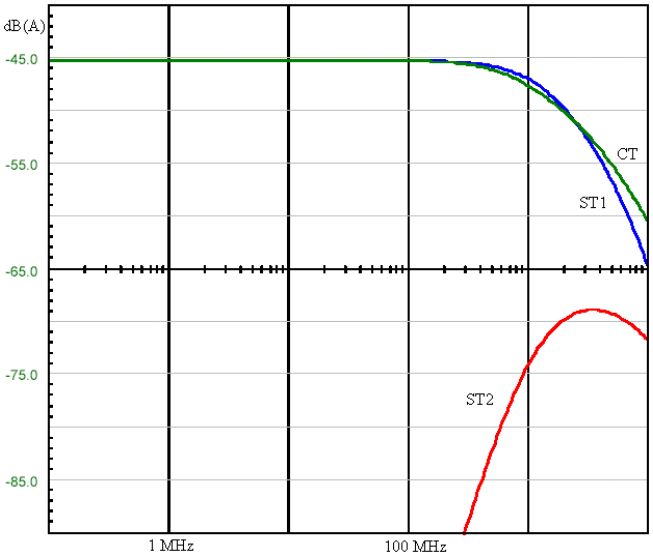

Fig. 6. Frequency domain simulation result for the output currents of the TX circuit considered in Section III, in dB with respect to 1 A.

domain results shown in Fig. 6 for 1 V applied to IN1. Below 200 MHz, the transadmittance for ST1 is about −45.2 dB(S) or 5.5 mS. The 3dB bandwidth for ST1 is about 1.5 GHz.

The relative error at the output of the balancing circuit, corresponding to $|\Delta i_C / i_1|$, where $|i_1|$ is the current through ST1, is about 0.030 up to 30 MHz and about 0.500 at 1 GHz.

IV. Application to a Pseudo-Differential Link

In this Section, we use the TX circuit of Section III in a 4-channel PDL in which the return conductor is used as a return path for the currents corresponding to the signals, as explained in Section II. This PDL comprises a 150-mm-long interconnection made of a coplanar-strips-over-return-conductor structure built in a printed circuit board, identical to the one used in [8, § 5].

This PDL is intended for the transmission of signals having a maximum bandwidth of 1 GHz. In this link, the signal outputs ST1 to ST4 and the common terminal CT of the 4-channel TX circuit studied in Section III are connected to the interconnection, the RX circuit and the termination circuit, as shown in Fig. 7. The termination circuit made of the resistors R11 to R14 is optimized to produce reduced reflections at the far-end, in line with the definition of the ZXnoise method [8]. The resistor R15 damps the resonances of the common-mode current.

The SPICE time domain simulation results shown in Fig. 8 and Fig. 9 use, for the interconnection, a sub-circuit created with SpiceLine [9].

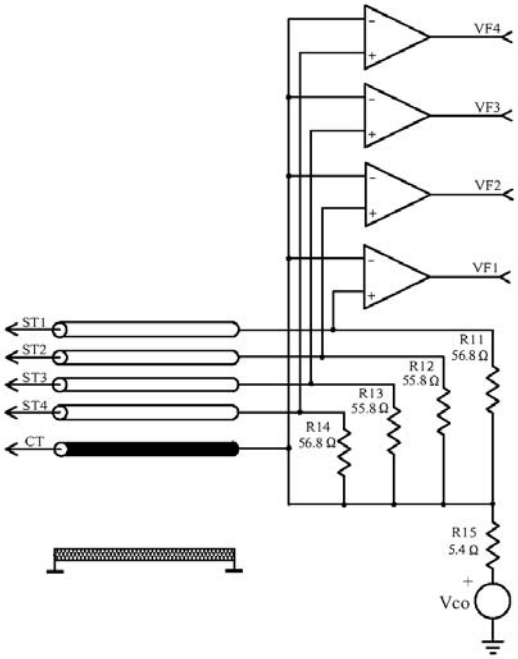

Fig. 7. The interconnection, the RX circuit and the termination circuit considered in Section IV. The 4 differential amplifiers have a gain of 1.

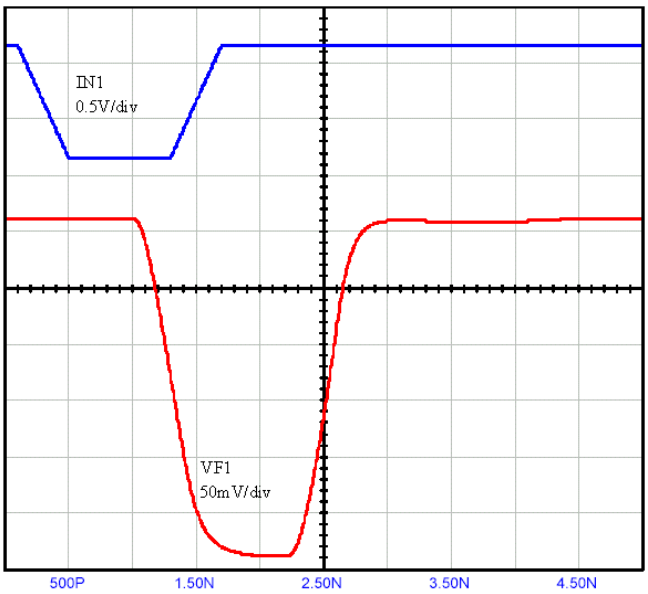

Fig. 8. Input signal at IN1 and transmitted voltage at VF1 versus time in ns.

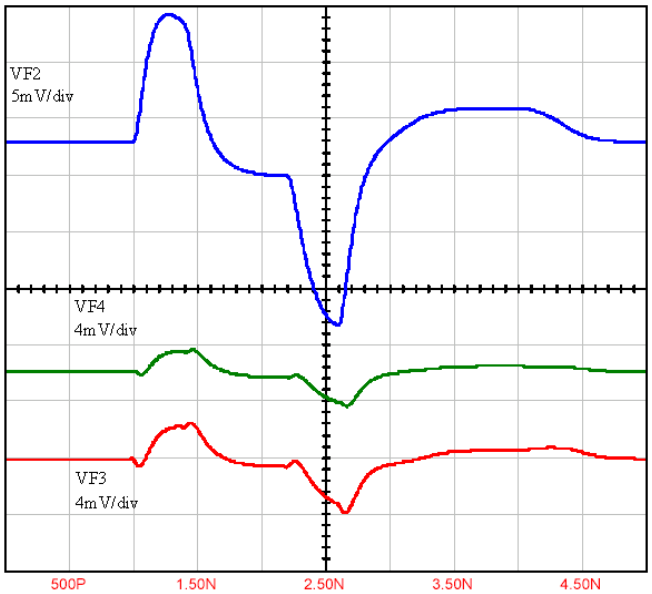

Fig. 9. Internal crosstalk voltages VF2, VF3 and VF4 versus time in ns.

The 1V pulse applied to the input IN1 has rise and fall times equal to 400 ps. Echo is not visible in Fig. 8. The internal crosstalk voltages shown in Fig. 9 do not exceed 16 mV peak, this value being compatible with binary signaling at the amplitude of 300 mV shown in Fig. 8.

V. Conclusion

Prior art pseudo-differential transmission schemes either use no termination (in which case large reflections occur) or the termination described in Section I, which creates variable common-mode currents. In the TX circuit considered in Sections III and IV, a balancing circuit reduces the variations of the common mode current flowing in the interconnection. A constant common-mode current would be obtained in an ideal implementation. The PDL implementing the ZXnoise method studied in Section IV consequently offers a good protection against external crosstalk, since a large part of the unwanted coupling between the PDL and nearby circuits is usually caused by the time variations of the common-mode current [10, ch. 11]. This reduced external crosstalk makes low-swing transmission possible.

This PDL comprises a termination circuit capable of low reflections. Low-swing and reduced reflections allow high-speed transmission.

References

[1] F. Yuan, *CMOS current-mode circuits for data communications*, New York, N.Y.:Springer, 2007.

[2] A. Carusone, K. Farzan, D.A. Johns, "Differential signaling with a reduced number of signal paths", *IEEE Trans. Circuits Syst. II*, vol. 48, No. 3, pp. 294-300, March 2001.

[3] S. Sidiropoulos, "Reducing coupled noise in pseudo-differential signaling", patent of the United States of America No. 7,099,395. Filed: November 7, 2000.

[4] T. Frodsham, "Multi-agent pseudo-differential signaling scheme", patent of the United States of America No. 6,195,395. Filed: March 18, 1998.

[5] W.F. Gunning, "Drivers and receivers for interfacing VLSI CMOS circuits to transmission lines", patent of the United States of America No. 5,023,488. Filed: March 30, 1990.

[6] *Design Considerations for Logic Products — Application Book — 1998*, Texas Instruments Deutschland, 1997.

[7] F. Broydé, E. Clavelier, "MIMO Series-Series Feedback Amplifiers", *IEEE Trans. Circuits Syst. II: Express Briefs*, Vol. 54, No. 12, Dec. 2007.

[8] F. Broydé, E. Clavelier, "A new pseudo-differential transmission scheme for on-chip and on-board interconnections", *Proc. of the CEM 08 Int. Symp. on Electromagnetic Compatibility*, Paris, May 2008, Available: http://www.eurexcem.com/zxnoisedef.htm.

[9] F. Broydé, E. Clavelier, L. Hoeft, "Comments on «A SPICE Model for Multiconductor Transmission Lines Excited by an Incident Electromagnetic Field»", *IEEE Trans. Electromagn. Compat.*, Vol. 38, No. 1, Feb. 1996, pp. 104-108.

[10] H.W. Ott, *Noise reduction techniques in electronic systems*, second edition, New York, N.Y.: John Wiley & Sons, 1988.