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Two Pseudo-Differential Transmitting Circuits Producing a Constant Common-Mode Current

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***Abstract* — This paper covers two possible designs for a new type of pseudo-differential transmitting circuit (TX circuit) such that signaling ideally produces no common-mode current variation. Here, the TX circuit terminals intended to be connected to the interconnection ideally behave as if the TX circuit was composed of a floating circuit and a two-terminal circuit element connected between the common terminal and ground. This is in contrast with conventional pseudo-differential TX circuits in which the generation of signals produces a variable return current flowing in the reference conductor. We provide simulation results based on the same CMOS technology for both designs. We then consider the implementation of one of these TX circuits in a pseudo-differential link. This link being capable of low reflections and an almost constant common-mode current, it offers a good protection against external crosstalk.**

I. Introduction

A pseudo-differential link (PDL) providing m channels [1, § 4.2.3] uses a multiconductor interconnection having m transmission conductors and a common conductor distinct from the reference conductor (ground). A PDL having $m = 4$ transmission conductors (numbered from 1 to 4) is shown in Fig. 1. The transmitting circuit (TX circuit) receives at its input the signals of the 4 channels of the source, and has $m + 1 = 5$ output terminals: one signal terminal (ST1 to ST4 in Fig. 1) connected to each one of the transmission conductors and one common terminal (CT) connected to the common conductor. The receiving circuit (RX circuit) has its 5 input terminals connected to the conductors of the interconnection, and its output terminals connected to the user.

PDLs are intended to provide a protection against *external crosstalk*, which corresponds to crosstalk between one or more channels of the PDL and other circuits, whereas *internal crosstalk* refers to crosstalk between the channels of the link. In a conventional PDL, the RX circuit ideally responds only to the m voltages between one of the transmission conductor and the common conductor. The routing and geometrical shape of all conductors of the interconnection being matched, it is expected that nearby circuits will induce practically equal disturbance voltages between each conductor and ground, so that noise cancellation occurs in the RX circuit. Thus, pseudo-differential signaling is intended to provide a protection against external crosstalk, using fewer terminals in the TX circuit and RX circuit than differential signaling.

Many conventional PDLs do not use any termination [1] [2] [3]. Since some do, a termination circuit has been included in Fig. 1, but it may or may not be present. When a termination circuit is present, it is typically made of grounded resistors [4] or of resistors connected to a power supply voltage, e.g. when integrated circuits of the Gunning Transceiver Logic (GTL) family [5] are used.

In this paper, we consider a new type of TX circuit intended to be used in a PDL used for transmitting analog or digital signals.

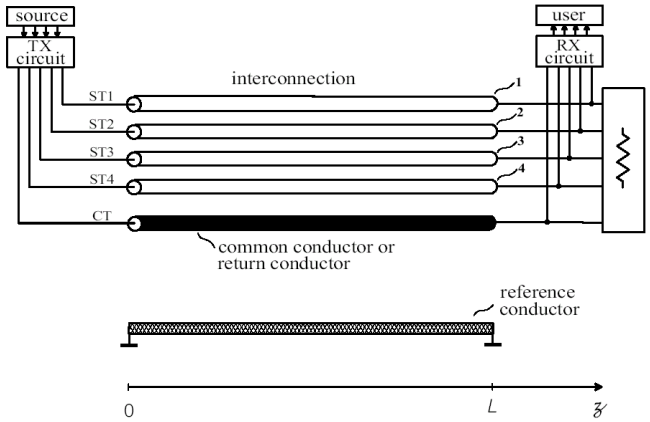

Fig. 1. A pseudo-differential link (PDL). The block containing the resistor symbol is a termination circuit which may or may not be present. The designation "common conductor" applies to conventional PDLs while "return conductor" applies to the PDLs considered in Sections II and V.

II. Definition of a New Type of TX Circuit

The new TX circuits are intended to be used with an interconnection having a structure which can be approximately modeled, for the propagation of signals in the PDL, as a $(m+1)$-conductor multiconductor transmission line (MTL). This result can be obtained when the shape of the common conductor is such that it in a way shields the transmission conductor from ground [6]. In this case, the "common conductor" shall be referred to as "return conductor", as shown in Fig. 1, because this configuration implies that this conductor should be used as a return path for the currents corresponding to the signals.

For any integer j such that $1 \le j \le m$, let us use i_j to denote the current flowing out of the signal terminal (ST) number j. Let us use i_C to denote the current flowing out of the common terminal (CT). Using the return conductor as a return path for the currents corresponding to the signals implies that the TX circuit does not cause significant variations of the common-mode current $i_1 + ... + i_m + i_C$. In order to be compatible with this definition of the new type of TX circuit, a TX circuit must, for the interconnection, approximately behave as if the TX circuit was composed of a floating circuit and a two-terminal circuit element connected between the CT and ground, the floating circuit having exactly $m + 1$ terminals connected to the m STs and the CT.

The corresponding equivalent circuit is shown in Fig. 2, for $m = 4$, in the special case where this two-terminal circuit element is composed of an impedor (i.e. a passive linear two-terminal circuit element) of admittance Y_D and a current source delivering a current i_{C0}. Since this current source is the only cause, within the TX circuit, of a possible common-mode current, i_{C0} must be a constant current. The case $Y_D = \infty$ corresponds to a TX circuit using ground as CT. In this case, the TX circuit is a standard line driver. An ideal new TX circuit corresponds to

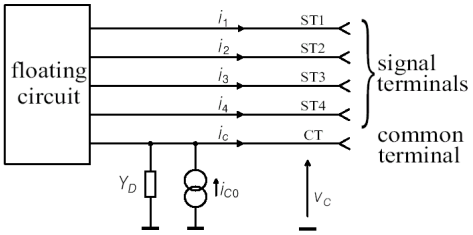

Fig. 2. Ideal circuit seen by the interconnection looking into the TX circuit.

the equivalent circuit of Fig. 2, in the case where Y_D is finite. In practice, Y_D might range between 1 mS and 1 S to obtain the lowest external crosstalk.

Let us use v_C to denote the voltage between the CT and ground. According to Fig. 2, we want that, when the TX circuit is in the activated state, at a given frequency $f \neq 0$

$$i_C \approx -\sum_{\alpha=1}^{m} i_\alpha - Y_D v_C \qquad (1)$$

Since no part of a practical TX circuit is floating, the TX circuit comprises a balancing circuit delivering i_C. The TX circuit is ideal if

$$i_C = -\sum_{\alpha=1}^{m} i_\alpha - Y_D v_C \qquad (2)$$

If we want to measure the admittance Y_D of an ideal linear interfacing device, Fig. 2 shows that we may apply any voltages or currents to the STs and the CT, as long as the voltage between the CT and ground is measured and the common-mode current is determined.

If the TX circuit is not assumed to be ideal, Y_D is clearly not uniquely defined by (1) alone. Consequently, in this case, the value measured for Y_D depends on the voltages or currents applied to the STs. However, for a given configuration, we will define Y_D as the ratio of the common-mode current to a voltage applied between the CT and ground *in this configuration*. Y_D being now uniquely defined in a given configuration, the error at the output of the balancing circuit in this configuration may be defined, at a given frequency $f \neq 0$, as

$$\Delta i_C = i_C + \sum_{\alpha=1}^{m} i_\alpha + Y_D v_C \quad , \qquad (3)$$

this error being zero when the TX circuit is ideal. Consequently, we may consider that the common-mode current contains a legitimate part $-Y_D v_C$ and an illegitimate part Δi_C.

III. First Pseudo-Differential TX Circuit

A first embodiment of the new type of TX circuit is made, for each channel, of a single transistor phase splitter driving the inputs of two current mirrors of opposite polarity. The resulting circuit for $m = 3$ channels is shown in Fig. 3. When the inputs (IN1, IN2 and IN3) are grounded, the TX circuit is in the deactivated state (high impedance state). When the inputs provide the signals and a suitable biasing, the signal terminals (ST1, ST2 and ST3) source the output currents i_1, i_2 and i_3. The common terminal (CT) would sink $-i_C = i_1 + i_2 + i_3$ in an ideal implementation. In this activated state, the NMOS current mirrors (M4-M5, etc) clearly form the balancing circuit mentioned in Section II. At low frequencies, the error at the output of the balancing circuit can only be caused by non-ideal current mirrors. We note that the output admittance of the PMOS current mirrors (M2-M3, etc) is by itself a departure from the ideal equivalent circuit of Fig. 2, unlike the output admittance of the NMOS current mirror.

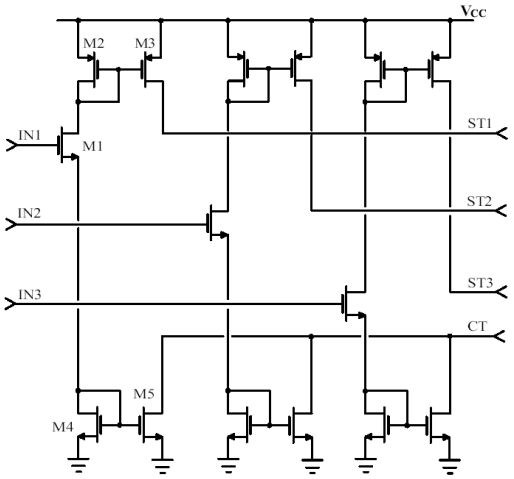

Fig. 3. A first pseudo-differential TX circuit, for $m = 3$.

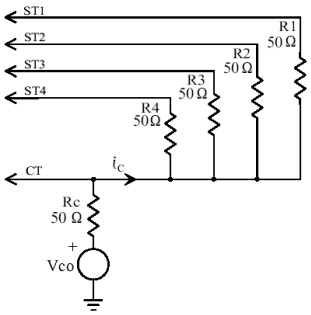

Fig. 4. Test circuit used for the assessment of the 4-channel TX circuits discussed in Section III and in Section IV.

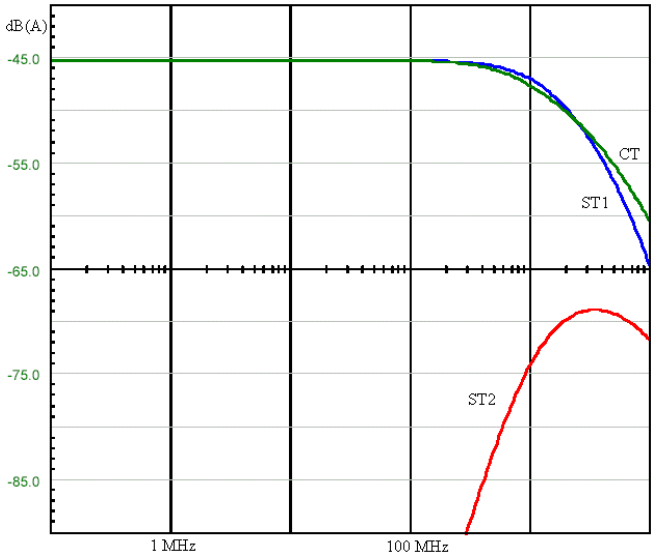

Fig. 5. Frequency domain simulation result for the output currents of the TX circuit considered in Section III, in dB with respect to 1 A.

We have simulated a 4-channel version of this circuit in a configuration in which the signal outputs ST1 to ST4 and the CT are connected to the test circuit shown in Fig. 4, the current i_C being measured at the point shown in Fig. 4 (consequently, the damping resistor Rc and the biasing voltage source Vco are now regarded as a part of the TX circuit). We have used the standard transistors of a 0.5-

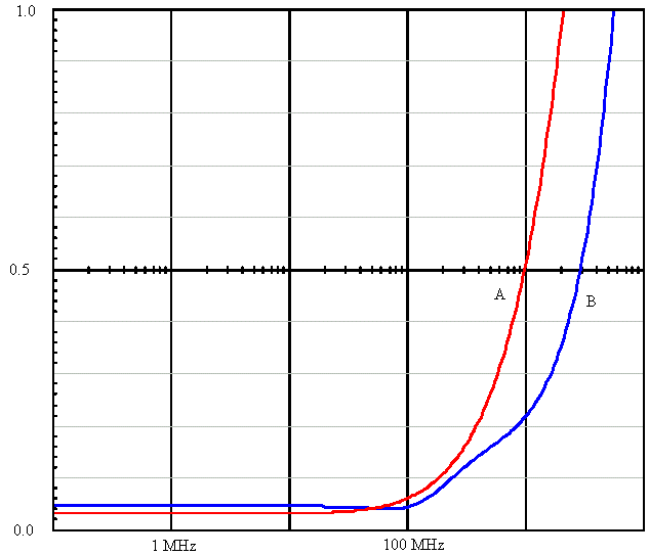

Fig. 6. Relative error for the 4-channel TX circuits of Section III (curve A) and Section IV (curve B).

µm CMOS process for which the propagation delay of two-transistor CMOS push-pull inverters is about 100 ps in a ring oscillator. We used W/L = 100/0.6 for the input transistors (M1, etc) and W/L = 200/0.6 for all other transistors. For a biasing such that all MOSFETs operate in the saturation regime (V_{CO} of Fig. 4 is 3/10 of the power supply voltage V_{CC}), we obtain the small-signal frequency domain results shown in Fig. 5 for 1 V applied to IN1. Below 200 MHz, the transadmittance for ST1 is about −45.2 dB(S) or 5.5 mS. The 3dB bandwidth for ST1 is about 1.5 GHz.

The relative error at the output of the balancing circuit, corresponding to the ratio $|\Delta i_C/i_1|$, where $|i_1|$ is the current through ST1, is shown in Fig. 6.

IV. Second Pseudo-Differential TX Circuit

The second new type of TX circuit uses one differential pair per channel to obtain current swings of opposite phase, as shown in Fig. 7 for m = 3 channels. When the TX circuit is activated, the biasing circuit comprising M4, M5 and M6 is such that the current sunk by the tail transistors (M3, etc) is twice the current sourced by the output transistors of the PMOS current source (M7, etc). In this manner, the quiescent current through the STs (ST1, ST2 and ST3) is zero, in an ideal implementation. The differential pairs' transistors connected to the CT form a balancing circuit.

As in Section III, we have simulated a 4-channel version of this circuit in a configuration using the test circuit shown in Fig. 4, the current i_C being measured at the point shown in Fig. 4. Our simulation uses the same transistors as the one used in Section III. We used W/L = 100/0.6 for the transistors of the differential pairs (M1-M2, etc), W/L = 200/0.6 for the tail transistors (M3, etc) and W/L = 300/0.6 for the output transistors of the PMOS current source (M7, etc). For a biasing such that all MOSFETs operate in the saturation regime (V_{CO} of Fig. 4 is equal to the power supply voltage V_{CC}), we obtained the small-signal frequency domain results shown in Fig. 8 for 1 V applied to IN1. Below 800 MHz, the transadmittance for ST1 is about −46.9 dB(S) or 4.5 mS. The 3dB bandwidth for ST1 is about 4.5 GHz. The relative error $|\Delta i_C/i_1|$ at the output of the balancing circuit is shown in Fig. 6.

This second pseudo-differential TX circuit provides a wider bandwidth than the first design of Section III and a lower relative error

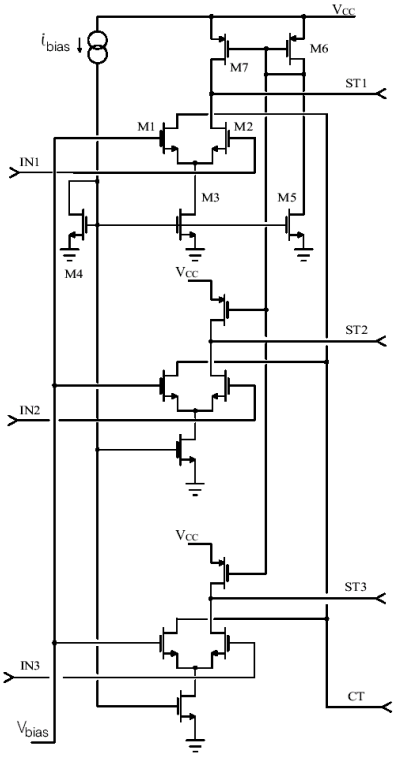

Fig. 7. A second 3-channel TX circuit.

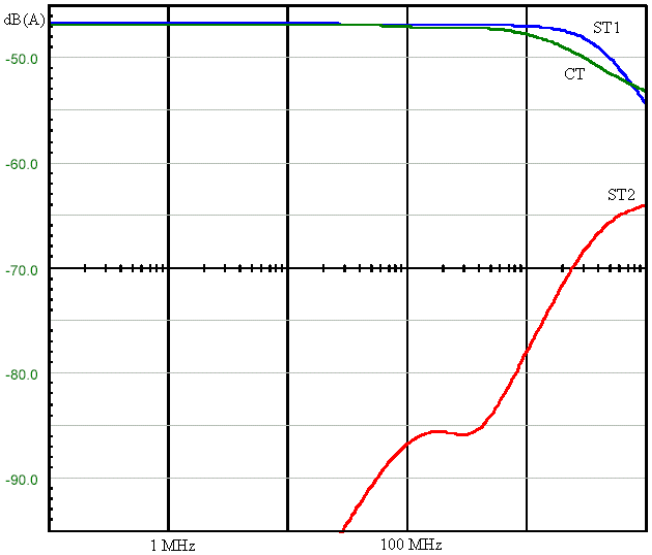

Fig. 8. Frequency domain simulation result for the output currents of the TX circuit considered in Section IV, in dB with respect to 1 A.

at the output of the balancing circuit, above 60 MHz. However, a comparison of Fig. 5 and 8 shows that it has lower crosstalk performances below 500 MHz.

V. Application to a Pseudo-Differential Link

In this Section, we implement a TX circuit producing a reduced common-mode current in a 4-channel PDL in which the return conductor is used as a return path for the currents corresponding to the signals, as explained in Section II. This PDL comprises a 150-mm-long interconnection made of a coplanar-strips-inside-return-conductor

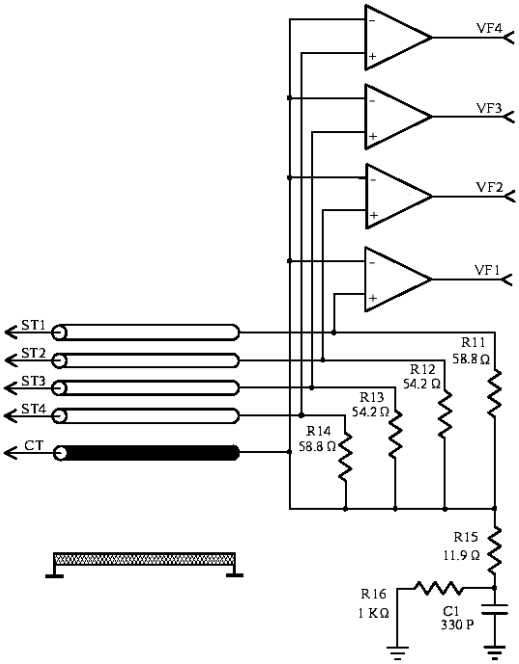

Fig. 9. The interconnection, the RX circuit and the termination circuit considered in Section V. The 4 differential amplifiers have a gain of 1.

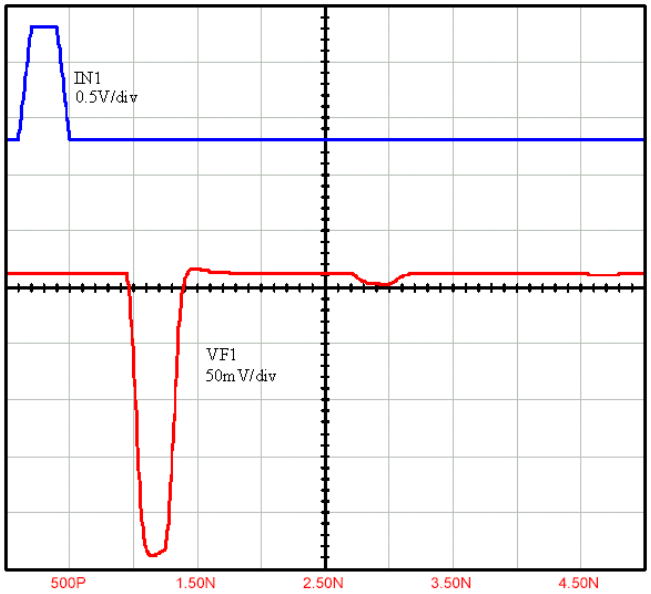

Fig. 10. Input signal at IN1 and transmitted voltage at VF1 versus time in ns.

structure built in a printed circuit board using the high-density interconnection technology, for the characteristics given in [6, § IV].

This PDL is intended for the transmission of signals having a maximum bandwidth of 4 GHz. In this link, the signal outputs ST1 to ST4 and the CT of the 4-channel TX circuit studied in Section IV are connected to the interconnection. At the near-end, a 50 Ω resistor connected between the CT and Vcc provides biasing. The configuration at the far-end is shown in Fig. 9: the termination circuit made of R11 to R14 reduces reflections, while R15, R16 and C1 damp the resonances of the common-mode current.

The SPICE simulation results shown in Fig. 10 and 11 use, for the interconnection, a sub-circuit created with SpiceLine [7]. The 1V pulse

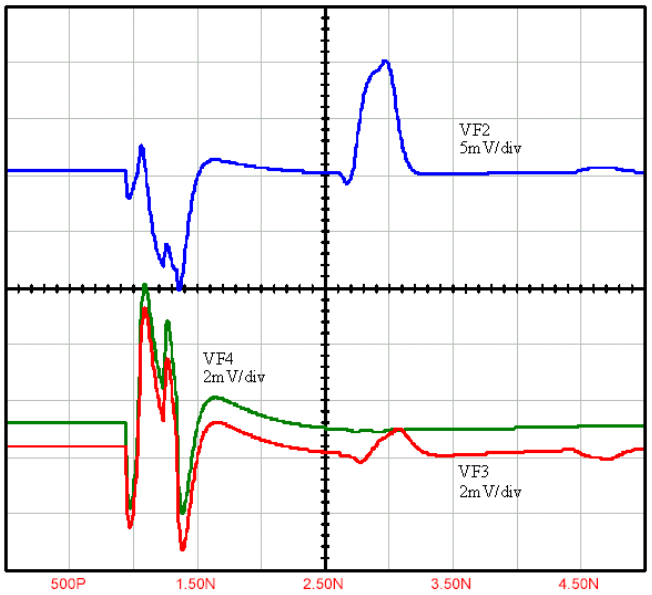

Fig. 11. Internal crosstalk voltages VF2, VF3 and VF4 versus time in ns.

applied to the input IN1 has rise and fall times equal to 100 ps. Echo is small in Fig. 10. The internal crosstalk voltages shown in Fig. 11 do not exceed 11 mV peak, this value being compatible with binary signaling at the amplitude of about 250 mV shown in Fig. 10.

VI. Conclusion

Prior art pseudo-differential transmission schemes either use no termination (in which case large reflections occur) or the termination described in Section I, which creates variable common-mode currents. The PDL described in Section V uses a special design for the interconnection termed ZXnoise [6]. It also uses a TX circuit and a termination circuit such that reflections are kept low and the common-mode current is practically constant (or zero). This PDL consequently offers a good protection against external crosstalk, since a large part of the unwanted coupling between the PDL and nearby circuits is usually caused by the time variations of the common-mode current [8, ch. 11].

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