Multichannel Pseudo-Differential Links

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***Abstract* — In this paper, we study multichannel pseudo-differential transmission schemes which use a common conductor or a return conductor. Combining 4 architectures with compatible types of termination circuit, we find that 12 multichannel pseudo-differential transmission schemes are possible. They provide a reduced external crosstalk compared to multiple single-ended links, using fewer conductors than multiple differential links.**

I. Introduction

A simple single-ended link is shown in Fig. 1. In this link, the signal produced by a single-port source is the input of a transmitting circuit (TX circuit). The output signal of a receiving circuit (RX circuit) is delivered to the user. An interconnection conveys the signal from the output of the TX circuit, at the near-end, to the input of the RX circuit, at the far-end. Here, the reference conductor (ground) is used for the return current produced by the currents flowing on the transmission conductor (TC) of the interconnection. Other circuits built on the same chip, multi-chip module (MCM), system in package (SiP) or printed circuit board (PCB) also use the reference conductor as a return path, for signal transmission and/or power feeding. Thus, significant common resistance and mutual inductance exist between these other circuits and the signal path formed by the TC and the reference conductor. This is a major cause of crosstalk between the link and such other circuits [1, § 4.2].

A simple pseudo-differential link (PDL) is shown in Fig. 2, where the interconnection is made of a TC and a common conductor and where the RX circuit is a differential amplifier such that the signal delivered to the user is mainly determined by the voltage between the TC and the common conductor. In this PDL, the common conductor is distinct from the reference conductor, even though the common conductor is grounded at the near-end, close to the TX circuit. Thus, the common resistance is canceled and the mutual inductance is effectively reduced between the signal path and said other circuits [1, § 4.6]. Consequently, the PDL shown in Fig. 2 is protected against crosstalk, with little additional hardware compared to Fig. 1 and less hardware than a differential link.

Pseudo-differential signaling may be extended to multi-channel links. This paper is about PDLs providing $m \geq 2$ channels for sending analog or digital signals, using an interconnection having a number $n \geq m$ of TCs and one common conductor distinct from the reference conductor [2, § 4.2.3] [3]. In this context, crosstalk between the different channels shall be referred to as *internal crosstalk* and crosstalk with other circuits shall be referred to as *external crosstalk*.

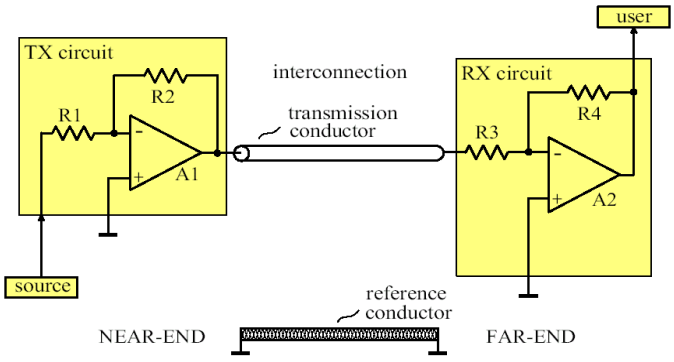

Fig. 1. A simple single channel single-ended link.

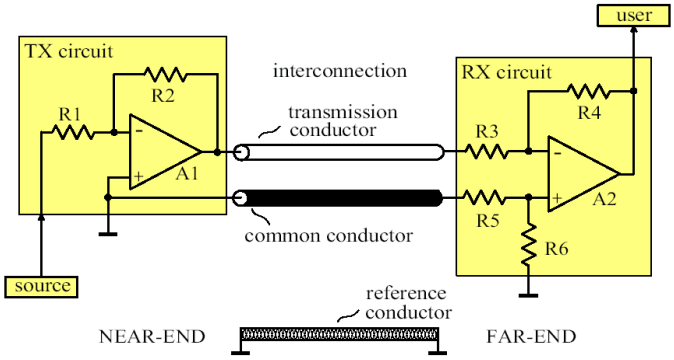

Fig. 2. A simple single channel pseudo-differential link (PDL).

Like the single-channel PDL shown in Fig. 2, the m-channel PDL provides a protection against external crosstalk because the output signals of the RX circuit are mainly determined by the voltages between the TCs and the common conductor. For m channels, a PDL might use only $m + 1$ conductors (in the case $n = m$) instead of $2m$ conductors for m differential links.

Several authors have introduced other multichannel transmission schemes, in which one or more of the output signals of the RX circuit are mainly determined by the voltages between two TCs, sometimes with the addition of a code maintaining a constant current [3] [4] [5] [6] [7]. Even though some such transmission schemes are sometimes referred to as pseudo-differential, they are not considered in this paper.

Four PDL architectures are presented and briefly discussed in Section II. The types of termination circuits which may be used to reduce reflections are presented in Section III. The suitability of interconnection-ground structures for a given type of termination circuit is addressed in Section IV, and suitable models are presented in Section V. Two examples are presented in Section VI. The 12 pseudo-differential transmission schemes which may be used are reviewed in the conclusion.

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II. The Four Possible PDL Architectures

We have identified 4 useful PDL architectures: PDL with voltage-driven common conductor (VDCC), PDL using common terminal switching circuits (SW circuits), unidirectional PDL operating at constant common-mode current (CCMC) and bidirectional PDL operating at CCMC. In cases where the common conductor is used as a return path for the currents corresponding to the signals, the common conductor may be referred to as *return conductor*.

A PDL with VDCC, providing $m = 4$ channels, is shown in Fig. 3. This PDL uses an interconnection having $n = 4$ TCs (numbered from 1 to 4). At the far-end of this unidirectional PDL, the termination circuit may or may not be present. At the near-end, close to the TX circuit, the common conductor is connected to a low impedance node presenting an open-circuit voltage e_{CC} and an internal impedance Z_{CC}. This node could be ground ($e_{CC} = 0$ V and $Z_{CC} = 0$ Ω). If, for instance, the PDL is intended for digital signals and built using integrated circuits of the Gunning Transceiver Logic (GTL) family, e_{CC} could advantageously be a reference voltage generated from the so-called "termination voltage", usually denoted by V_{TT}.

If bidirectional operation is desired, the architecture of Fig. 3 cannot be used since at most one low impedance node may be connected to the common conductor of a PDL, at a given time. However, a PDL using SW circuits, shown in Fig. 4, may be used. In this type of PDL, when one of the TX circuits is in the activated state, the nearest SW circuit is in the closed state, in which it couples the common conductor to a low impedance node, while the other SW circuit(s) is(are) in the open state. Thus, at a given point in time, the PDL of Fig. 4 is equivalent to the PDL shown in Fig. 3. One or more of the termination circuits shown in Fig. 4 may or may not be present. More than two TX circuits could be used along the interconnection, but only one TX circuit can be in the activated state at a given time.

The PDL with VDCC (Fig. 3) and the PDL using SW circuits (Fig. 4) may use conventional voltage-mode TX circuits (which produce signals in the form of voltages referenced to ground) or current-mode TX circuits [2] if a termination circuit is present.

A TX circuit may comprise a balancing circuit such that a CCMC flows in the interconnection [8]. Such a TX circuit has a "common terminal" connected to the return conductor. It may be used in a unidirectional PDL or in a bidirectional PDL such as the one shown in Fig. 5. Let us use i_j to denote the current flowing from the signal terminal number j of the TX circuit to the TC number j to which it is connected, and i_C to denote the current flowing from the common terminal of the TX circuit to the return conductor. The balancing circuit controls i_C in such a way that the TX circuit does not cause any significant variation of the common-mode current $i_1 + ... + i_n + i_C$. Thus, the balancing circuit provides a return path for the signal currents i_1 to i_n while not requiring a connection of the return conductor to a low-impedance node. Consequently, such TX circuits are compatible with simultaneous bidirectional transmission (i.e. full duplex signaling) in PDLs.

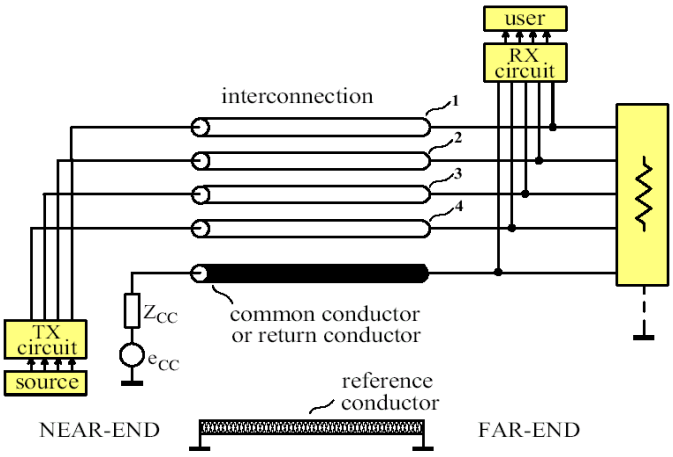

Fig. 3. Unidirectional multichannel PDL with voltage-driven common conductor or return conductor (VDCC). The block containing the resistor symbol is a termination circuit.

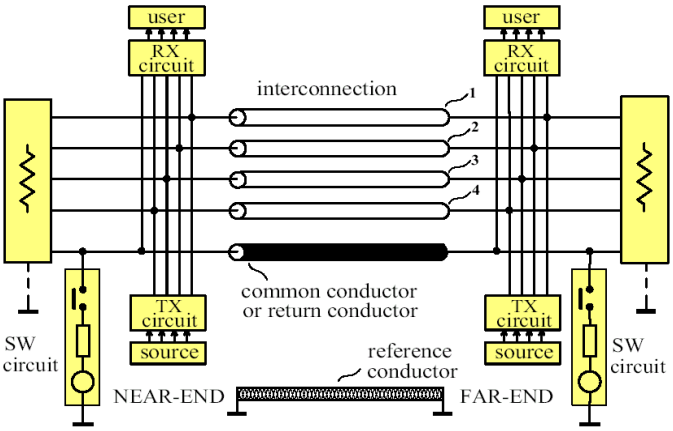

Fig. 4. Bidirectional multichannel PDL using common terminal switching circuits (SW circuits).

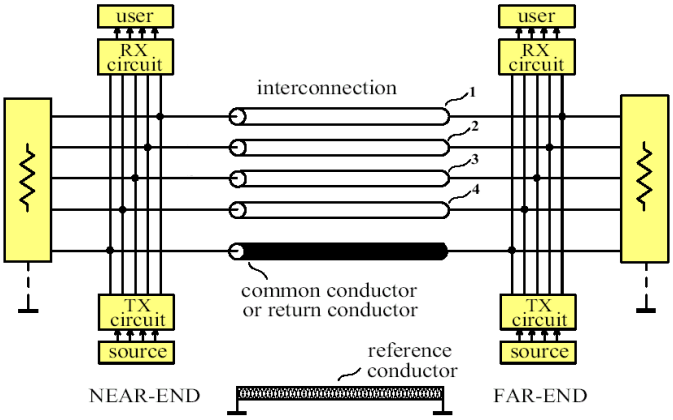

Fig. 5. Bidirectional multichannel PDL with TX circuits producing a constant common-mode current (CCMC).

III. Termination Circuits And The ZXNoise Method

No termination circuit is present in some PDLs with VDCC [2]. In PDLs using SW circuits, no termination circuit is required either. If no termination circuit is used in a PDL, reflections of signals occur and limit the available bandwidth for a given interconnection length.

Other PDLs with VDCC or PDLs using SW circuits use type 1 termination circuits [9]. By definition, a type 1 termination circuit has an impedance matrix with respect to ground, denoted by $\mathbf{Z}_{GT}$, and $\mathbf{Z}_{GT}$ is a diagonal matrix. Thus, a type 1 termination circuit may be made of grounded resistors, as shown in Fig. 6 for $n = 4$. The termination circuit may merely consist of the resistors R_1 to R_n connected to the TCs (TC1 to TC4 in Fig. 6). If we wish that the common conductor operates in the same configuration as the TCs, a resistor R_D connected to the common conductor (CC in Fig. 6) may also be used. Such a termination circuit uses the reference conductor for the return current produced by the currents flowing on the TCs. The reference conductor belonging to the signal path, this type 1 termination circuit will produce an unwanted coupling between other circuits using the reference conductor as a return path and the signal path formed by the TCs, the common conductor and the reference conductor. If the termination circuit shown in Fig. 6 is used in the architectures of Fig. 3 or Fig. 4, balancing out the external crosstalk in the RX circuit is theoretically possible in some cases. In practice however, this termination circuit will decrease the effectiveness of the external crosstalk reduction.

By definition, the ZXnoise method uses type 2 or type 3 termination circuits which behave as if they were not connected to ground, so that they are characterized by an impedance matrix with respect to the return conductor, denoted by $\mathbf{Z}_{RL}$ [10]. $\mathbf{Z}_{RL}$ is a matrix of size $n \times n$, $\mathbf{Z}_{RL}$ being a diagonal matrix in the case of a type 2 termination circuit, or a non-diagonal matrix in the case of a type 3 termination circuit. In the ZXnoise method, the common conductor may be called a return conductor since it is used as a return path for the currents flowing on the TCs.

In Fig. 7, a type 2 termination circuit for $n = 4$ consists of the resistors R_1 to R_4 each connected between one of the TCs (TC1 to TC4) and the return conductor (RC in Fig. 7). In Fig. 8, a type 3 termination circuit for $n = 4$ consists of the resistors R_1 to R_4 used as in Fig. 7, and of the resistors R_{12}, R_{13}, R_{14}, R_{23}, R_{24} and R_{34} each connected between two TCs. In Fig. 7 and Fig. 8, we use a damping device connected between the return conductor and ground, in the form of a resistor R_D, for damping the resonances of the return conductor with respect to ground. The damping resistor R_D is not regarded as a part of the termination circuit. Since the damping device is not part of the termination circuit (it is not part of the intended signal path), type 2 and type 3 termination circuits are floating and they do not have an impedance matrix with respect to ground. If a damping device is present, the combination of a type 2 or type 3 termination circuit and the damping device has an impedance matrix with respect to the return conductor and an impedance matrix with respect to ground, both being of size $(n + 1)\times(n + 1)$.

Type 2 and type 3 termination circuits do not place the reference conductor in the signal path. Thus, they do not introduce unwanted couplings between other circuits using the reference conductor as a return path and the signal path formed by the TCs and the return conductor. Consequently, type 2 and type 3 termination circuits do not degrade external crosstalk.

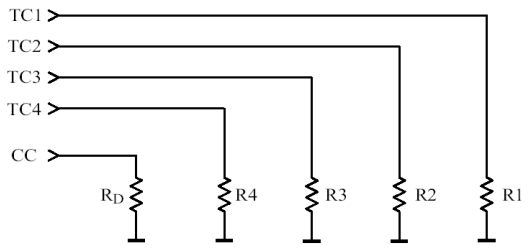

Fig. 6. A type 1 termination circuit, made of grounded resistors. CC is the common conductor.

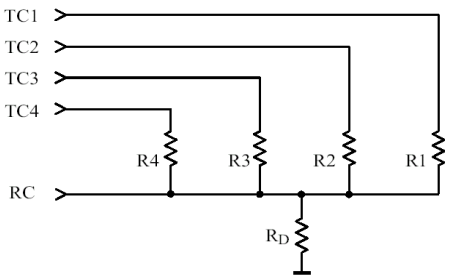

Fig. 7. A type 2 termination circuit and a damping resistor R_D. RC is the return conductor.

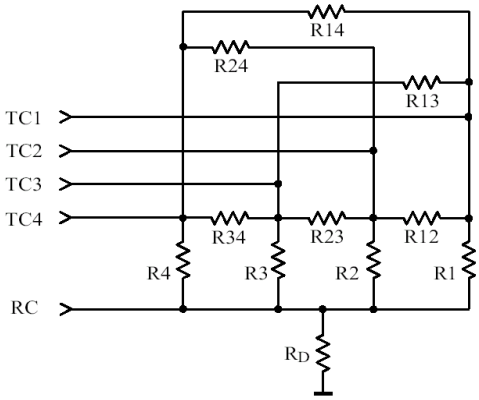

Fig. 8. A type 3 termination circuit and a damping resistor R_D. RC is the return conductor.

IV. Structure of the Interconnection

The interconnection comprises the n TCs and the common/return conductor (the reference conductor is not considered part of the interconnection). The termination circuits are primarily intended to reduce reflections. Consequently, the type(s) of termination circuit which may be used in a given link depend(s) on the characteristics of the interconnection.

A type 1 termination circuit absorbs the incoming power of the signal using resistance between the TCs and ground. It will operate as intended if (condition A) the electric and magnetic fields of the signals are mainly located between the TCs and ground. In this case, the return current caused by signal propagation flows mainly in the reference conductor. This is for instance obtained in the two interconnection-ground structures shown in Fig. 9, provided that the distances between nearby

conductors of the interconnection are large enough compared to the distances between each conductor of the interconnection and the reference conductor. Here, propagation takes place in the whole interconnection-ground structure, which must be modeled as a $(n+2)$-conductor multiconductor transmission line (MTL).

Type 2 and type 3 termination circuits (floating termination circuits) absorb the incoming power of the signal using resistance between the TCs and the return conductor. They will operate as intended if (condition B) the electric and magnetic fields of the signals are mainly confined between the TCs and the return conductor. In this case, the return current caused by signal propagation flows mainly in the return conductor. This is for instance obtained if one of the interconnection-ground structures shown in Fig. 10 is used with floating termination circuits. This is because, in Fig. 10, the return conductor may clearly behave as an electromagnetic screen [10]. Thus, propagation takes place in the interconnection alone, which may be modeled as a $(n+1)$-conductor MTL at the design stage, as explained below in Section V.

However, allocating one or more conducting layers or metallization levels to the return conductor is not necessary to meet the condition B: in the interconnection-ground structures shown in Fig. 11, the return conductor is made of multiple traces which share the same layer as the TCs, so that a two-layer structure and a single-layer structure have been obtained. These structures must clearly be proportioned and used carefully to obtain the desired fulfilment of the condition B.

V. Models for the Interconnection

Each interconnection-ground structures considered in Section IV may be modeled as a $(n+2)$-conductor MTL. This model uses, at a given abscissa z along the interconnection:

- for any integer α such that $1 \le \alpha \le n$, the current i_α flowing on the TC number α ;
- the current flowing on the common or return conductor, denoted by i_{n+1} ;
- for any integer α such that $1 \le \alpha \le n$, the voltage between the TC number α and the reference conductor, denoted by $v_{G\alpha}$;
- the voltage between the common or return conductor and the reference conductor, denoted by $v_{G\,n+1}$.

We define the column-vector $\mathbf{I}_G$ of the natural currents $i_1,\ldots, i_{n+1}$ and the column-vector $\mathbf{V}_G$ of the natural voltages referenced to ground $v_{G1},\ldots, v_{G\,n+1}$. For this $(n+2)$-conductor MTL model using natural voltages referenced to ground and natural currents as variables, the telegrapher's equations are:

$$\begin{cases} \dfrac{d\,\mathbf{V}_G}{dz} = -\mathbf{Z}_G\,\mathbf{I}_G \\ \dfrac{d\,\mathbf{I}_G}{dz} = -\mathbf{Y}_G\,\mathbf{V}_G \end{cases} \qquad (1)$$

where $\mathbf{Z}_G$ and $\mathbf{Y}_G$ are the per-unit-length (p.u.l.) impedance matrix with respect to ground, and the p.u.l. admittance matrix with respect to ground, respectively. $\mathbf{Z}_G$ and $\mathbf{Y}_G$ are symmetric matrices of size $(n+1)\times(n+1)$.

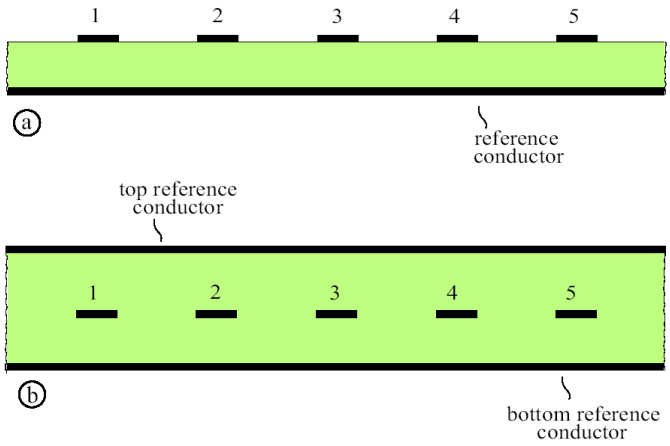

Fig. 9. Two possible cross-sections for an interconnection-ground structure used with type 1 termination circuits, where 1 to 4 are the TCs and where 5 is the common conductor.

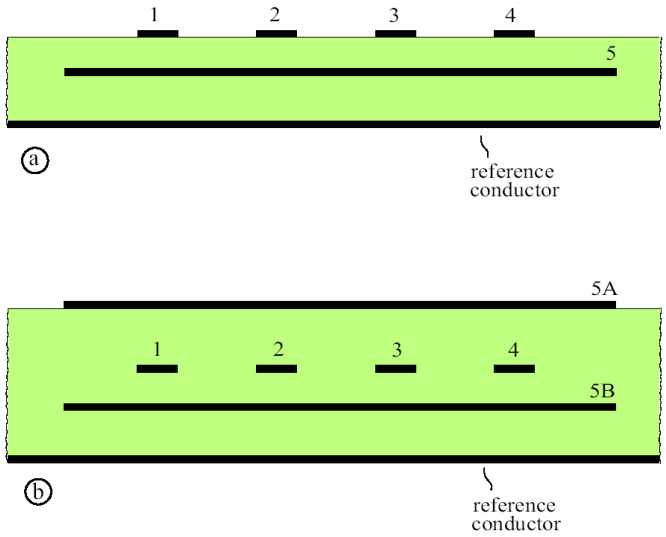

Fig. 10. Two possible cross-sections for an interconnection-ground structure used with floating termination circuits, where 1 to 4 are the TCs, where 5 is the return conductor in *a* and where the return conductor in *b* is made of 5A and 5B, which must be sufficiently interconnected.

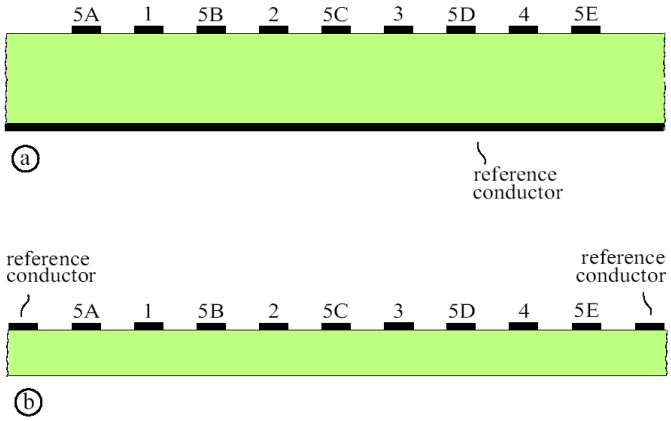

Fig. 11. Two possible cross-sections for an interconnection-ground structure used with floating termination circuits, where 1 to 4 are the TCs and where the return conductor is made of 5A to 5E, which must be sufficiently interconnected.

These equations are not very convenient for investigating PDLs, since, in a PDL, an RX circuit senses the natural voltages referenced to the return conductor, denoted by $v_{R1},..., v_{Rn}$, where $v_{R\alpha}$ is the voltage between the TC number α and the return conductor. We define the column-vector $\mathbf{I}_R$ of the natural currents $i_1,..., i_n$ and the column-vector $\mathbf{V}_R$ of the natural voltages referenced to the return conductor $v_{R1},..., v_{Rn}$, such that $v_{R\alpha} = v_{G\alpha} - v_{Gn+1}$ for $1 \le \alpha \le n$. The telegrapher's equations applicable to $\mathbf{I}_R$ and $\mathbf{V}_R$ in the case $n \ge 2$ use 2 additional variables and 6 new p.u.l. quantities. The additional variables are the common-mode current $i_{MC} = i_1 + ... + i_{n+1}$ and the common-mode voltage $v_{MC} = v_{Gn+1}$. The new p.u.l. quantities are [11]:

■ the p.u.l. impedance matrix with respect to the return conductor, a symmetric matrix of size $n \times n$ denoted by $\mathbf{Z}_R$, the p.u.l. transfer impedance vector, of size $n \times 1$ and denoted by $\mathbf{Z}_E$, and the external impedance, denoted by Z_{EE}, defined by

$$Z_{G\alpha\beta} = Z_{R\alpha\beta} + Z_{EE} - Z_{E\alpha} - Z_{E\beta} \tag{2}$$

$$Z_{Gn+1\alpha} = Z_{G\alpha n+1} = Z_{EE} - Z_{E\alpha} \tag{3}$$

and

$$Z_{Gn+1n+1} = Z_{EE} \quad ; \tag{4}$$

■ the p.u.l. admittance matrix with respect to the return conductor, a symmetric matrix of size $n \times n$ denoted by $\mathbf{Y}_R$, the p.u.l. transfer admittance vector, of size $n \times 1$ and denoted by $\mathbf{Y}_E$, and the external admittance, denoted by Y_{EE}, defined by

$$Y_{G\alpha\beta} = Y_{R\alpha\beta} \tag{5}$$

$$Y_{Gn+1\alpha} = Y_{G\alpha n+1} = Y_{E\alpha} - \sum_{\beta=1}^{n} Y_{R\alpha\beta} \tag{6}$$

and

$$Y_{Gn+1n+1} = Y_{EE} + \sum_{\alpha=1}^{n}\sum_{\beta=1}^{n} Y_{R\alpha\beta} - 2\sum_{\alpha=1}^{n} Y_{E\alpha} \tag{7}$$

where α and β are integers such that $1 \le \alpha \le n$ and $1 \le \beta \le n$ and where indices have been used to denote the entries of matrices and vectors. Using ${}^t\mathbf{X}$ to denote the transpose of $\mathbf{X}$, it can been shown that (1) is exactly equivalent to

$$\begin{cases} \dfrac{d\,\mathbf{V}_R}{dz} = -\mathbf{Z}_R\,\mathbf{I}_R + i_{MC}\,\mathbf{Z}_E \\ \dfrac{d\,\mathbf{I}_R}{dz} = -\mathbf{Y}_R\,\mathbf{V}_R - v_{MC}\,\mathbf{Y}_E \end{cases} \tag{8}$$

and

$$\begin{cases} \dfrac{d\,v_{MC}}{dz} = {}^t\mathbf{Z}_E\,\mathbf{I}_R - i_{MC}\,Z_{EE} \\ \dfrac{d\,i_{MC}}{dz} = -{}^t\mathbf{Y}_E\,\mathbf{V}_R - v_{MC}\,Y_{EE} \end{cases} \tag{9}$$

The equations (8) and (9) are valid for any pseudo-differential transmission scheme. In the case of interconnection-ground structures meeting the condition A, no simplification occurs in (2) to (9), so that it might be advisable to use (1) for the synthesis and the analysis of the PDL. In the case where one of the interconnection-ground structures shown in Fig. 10, meeting the condition B, is used with floating terminations, the return current caused by signal propagation flows mainly in the return conductor. The return conductor behaving as an electromagnetic screen, the p.u.l. transfer impedance vector $\mathbf{Z}_E$ and the p.u.l. transfer admittance vector $\mathbf{Y}_E$ are small, so that (8) may be replaced with

$$\begin{cases} \dfrac{d\,\mathbf{V}_R}{dz} = -\mathbf{Z}_R\,\mathbf{I}_R \\ \dfrac{d\,\mathbf{I}_R}{dz} = -\mathbf{Y}_R\,\mathbf{V}_R \end{cases} \tag{10}$$

and (9) is not needed for the synthesis stage since i_{MC} and v_{MC} are not intentionally excited by the PDL. Thus, propagation takes place in the interconnection alone, which may be modeled as a $(n + 1)$-conductor MTL [10].

At the design stage, using this $(n + 1)$-conductor MTL model instead of the $(n + 2)$-conductor MTL model allows us to compute an adequate $\mathbf{Z}_{RL}$ and to synthesize the corresponding type 2 or type 3 termination circuit, which does not degrade external crosstalk. This is the essence of the ZXnoise method.

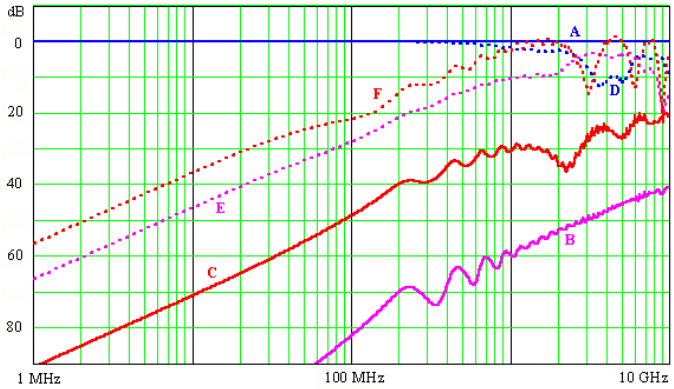

Fig. 12. Attenuations observed on the PDLs of Section VI. For the second PDL, measured on channel 2: attenuation of transmitted signal (curve A), lowest attenuation of far-end internal crosstalk when channel 3 or 4 are excited (curve B), attenuation of external crosstalk (curve C). For the first PDL, measured on TC number 2: attenuation of transmitted signal (curve D), lowest attenuation of far-end internal crosstalk when another TC is excited (curve E), attenuation of external crosstalk (curve F).

VI. Comparison of Two Links

We consider two PDLs providing $m = 4$ channels. Both PDLs use the VDCC architecture shown in Fig. 3 and a 0.3-m long interconnection-ground structure of the type shown in Fig. 10a (described in detail in the Section V of [11]). The first PDL uses type 2 termination circuits, like the PDLs considered in [10] and [11]. The second PDL uses type 3 termination circuits. At the far-end, both PDLs use a damping resistor, with $R_D = 10\ \Omega$.

The second PDL combines the ZXnoise method and the ZXtalk method [12, § VI], so that the design procedure of the ZXtalk method must be applied to (10) to obtain a type 3 termination circuit. More precisely, $\mathbf{Z}_{RL}$ must approximate the characteristic impedance matrix $\mathbf{Z}_{RC}$ derived from (10), in a suitable frequency band. In this second PDL, the propagation velocities being significantly different for the different modes, the "special ZXtalk method for completely degenerate interconnections" [12, § VIII] cannot be used, so that the TX circuit and the RX circuit must perform linear combinations of signals to allocate one propagation mode derived from (10) to

each channel. However, since these modes are not the exact propagation modes derived from (1) or from (8) and (9), some residual internal crosstalk is expected.

Figure 12 shows frequency domain simulation results based on (1), where the curves A, B and C are for the channels 2, 3 and 4 of the second PDL, and the curves D, E and F are for the first PDL. Compared to the latter, the channels 2, 3 and 4 of the new PDL have a reduced internal crosstalk suitable for fast signaling, and also a reduced external crosstalk. We found that the channel 1 of the new PDL, not considered in Fig. 12, is not suitable for fast signaling. The curves C and F of Fig. 12 show the attenuation of external crosstalk when the same noise is induced on every conductor in the TX circuit, in order to simulate simultaneous switching output (SSO) noise. The Fig. 13 shows time domain simulation results based on (1), for the first and the second PLD. The second PLD has a much lower internal crosstalk, at the cost of an increased complexity.

VII. Conclusion

A PDL may provide a reduced external crosstalk in m channels, using $m + 1$ conductors instead of $2m$ conductors for m differential links. The table I shows the different possible combinations of PDL architectures and types of termination circuit (type 0 referring to the absence of termination), and their novelty. A CCMC TX circuit needs a termination circuit which cannot be a type 1 termination circuit, because the required R_D would create internal crosstalk. All other combinations being of interest, we have identified 12 pseudo-differential transmission schemes, 9 of which are new.

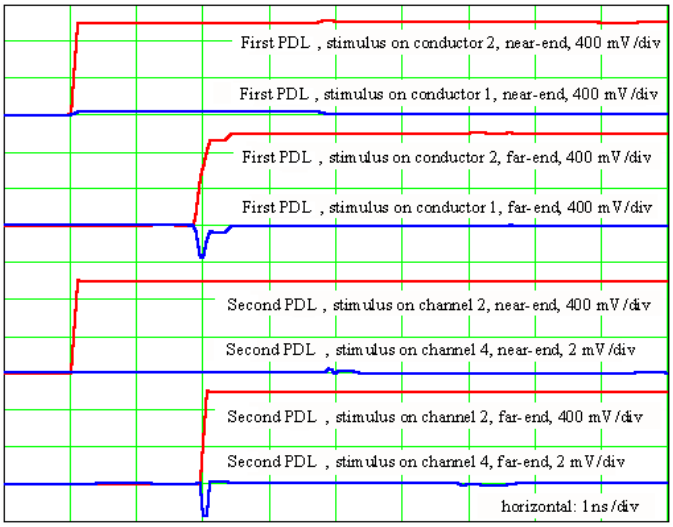

Fig. 13. Voltages in the PDLs considered in Section VI, measured on conductor 2 in the case of the first PDL or on channel 2 in the case of the second PDL, the stimulus being a 1V step having a 100 ps rise time. In the first PDL, conductor 1 is the one that produces the highest peak crosstalk voltage on conductor 2. In the second PDL, channel 4 is the one that produces the highest peak crosstalk voltage on channel 2.

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Table I. Possible Pseudo-Differential Transmission Schemes

Termination circuit	Architecture of the PDL			
	VDCC (unidirectional)	SW circuit (bidirectional)	Unidirectional CCMC	Bidirectional CCMC
Type 0	Prior Art [2, § 4.2] [3]	New		
Type 1	Prior Art [9]	New		
Type 2 (ZXnoise)	New	New	Recent [8] [10]	New
Type 3 (ZXnoise)	New	New	New	New