MIMO Series–Series Feedback Amplifiers

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***Abstract*—This brief defines a new type of multiple-input multiple-output (MIMO) amplifier. We present basic structures for this MIMO series–series feedback amplifier (MIMO-SSFA), and the basic design equations. We provide a detailed example showing how this MIMO-SSFA may be used as a transmitting circuit for multiconductor interconnections.**

***Index Terms*—Amplifiers, antenna array, crosstalk, feedback circuits, low-noise amplifier, multiple-input multiple-output (MIMO) systems.**

I. Introduction

THE RF front-end of a radio transmitter (respectively, receiver) connected to multiple antennas could use a multiple-input multiple-output (MIMO) power amplifier (respectively, MIMO low-noise amplifier) instead of multiple independent amplifiers. The transmitting circuit (respectively, receiving circuit) used for transmitting through a multiconductor interconnection could also use a MIMO amplifier instead of multiple independent line drivers (respectively, line receivers). The advantage of using a MIMO amplifier resides in the possibility of introducing controlled or needed couplings between channels.

In this brief, we consider a new type of linear MIMO amplifier having n inputs and n outputs, which may be used in several types of devices processing multiple input signals. A general theory of MIMO feedback amplifier is presented in [1, ch. 29], but the formalism of this theory is not explicitly used in this brief. Section II defines the MIMO series–series feedback amplifier (MIMO-SSFA). Section III provides design equations. Section IV explains the design of a 4-input and 4-output MIMO-SSFA used as a transmitting circuit for a multiconductor interconnection [2]. Section V shows additional capabilities of the MIMO-SSFA.

II. Definitions

A MIMO-SSFA providing $n \geq 3$ channels has $n+1$ input terminals (n signal input terminals numbered from 1 to n and ground) and $n+1$ output terminals (n signal output terminal numbered from 1 to n and ground). Fig. 1 shows a MIMO-SSFA, having $n = 4$ signal input terminals and n signal output terminals, comprising n active sub-circuits (ASCs) and a feedback network (FN). If j is an integer such that $1 \leq j \leq n$, Fig. 2 shows the ASC j having its sub-circuit input terminal I connected to the signal input terminal j and its sub-circuit output terminal O connected to the signal output terminal j.

Fig. 2 shows the input voltage e_j, the output voltage v_j and the voltage w_j between the sub-circuit common terminal C and ground. Fig. 2 also shows the current $i_{\mathrm{I}Aj}$ flowing into the sub-circuit input terminal, the current $i_{\mathrm{O}Aj}$ flowing into the sub-circuit output terminal, and the current $i_{\mathrm{C}Aj}$ flowing out of the sub-circuit common terminal. Each ASC is such that $i_{\mathrm{C}Aj}$ and $i_{\mathrm{O}Aj}$ depend on $e_j - w_j$. An ASC can be a single transistor or a more complex circuit possibly having connections to ground and/or to one or more power supplies, even though such connections are not shown. The FN has a grounded terminal and n other terminals each being connected to the sub-circuit common terminal of a different ASC. The FN presents a nondiagonal impedance matrix $\mathbf{Z}_{\mathrm{FB}}$, this impedance matrix being defined with respect to the reference terminal, and the FN produces a negative feedback. The name "MIMO-SSFA" used to designate this amplifier is a consequence of the fact that the negative feedback used in Fig. 1 can be considered as a generalization of series–series feedback.

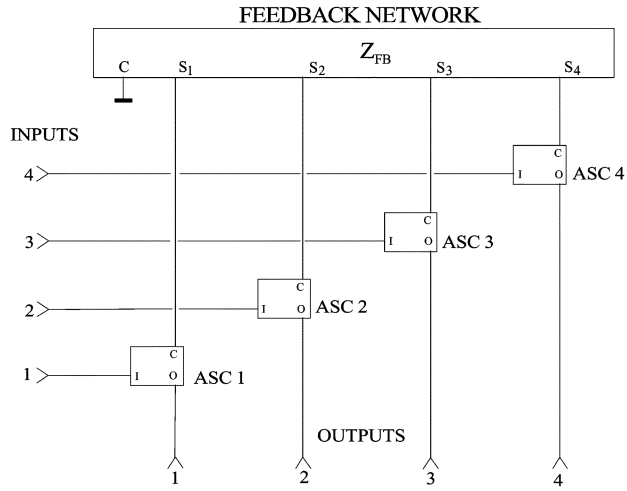

Fig. 1. MIMO-SSFA.

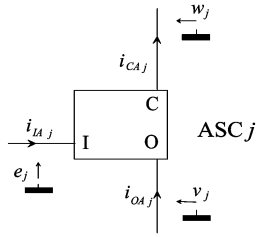

Fig. 2. ASC of the MIMO-SSFA.

The distinctive feature of a MIMO-SSFA is that the n inputs and n outputs are inherently coupled by a $(n+1)$-terminal FN. Consequently, we further require that the FN cannot be split into two uncoupled sub-networks, or, equivalently that the MIMO-SSFA cannot be split into two uncoupled amplifiers.

If we had not required that $n \geq 3$, a differential pair connected to a finite degeneration resistor could have been regarded as a 2-input and 2-output MIMO-SSFA. Many useful multiple-

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input circuits comprising a plurality of differential pairs are not MIMO-SSFA as defined above, for instance the differential difference amplifier (DDA) [3], the fully balanced DDA [4] and the universal opamp [5]. The MIMO amplifier invented by Yamaji *et al.* [6] is not a MIMO-SSFA either, since it does not allow the definition of the impedance matrix of a FN.

Let us define the input current i_{Ij} flowing into the signal input terminal j and the input voltage v_{Ij} between the signal input terminal j and ground. We also define the column-vector $\mathbf{I}_I$ of the input currents $i_{I1},\ldots,i_{In}$, and the column-vector $\mathbf{V}_I$ of the input voltages $v_{I1},\ldots,v_{In}$. Let us define the output current i_{Oj} flowing into the signal output terminal j and the output voltage v_{Oj} between the signal output terminal j and ground. We also define the column-vector $\mathbf{I}_O$ of the output currents $i_{O1},\ldots,i_{On}$, and the column-vector $\mathbf{V}_O$ of the output voltages $v_{O1},\ldots,v_{On}$.

For small signals, at a given quiescent operating point, the MIMO-SSFA is characterized, in the frequency domain, by the following two equations:

$$\mathbf{I}_I = \mathbf{Y}_I\mathbf{V}_I + \mathbf{Y}_R\mathbf{V}_O \tag{1}$$

$$\mathbf{I}_O = \mathbf{Y}_T\mathbf{V}_I + \mathbf{Y}_O\mathbf{V}_O \tag{2}$$

where we can refer to$\mathbf{Y}_I$ as the "short-circuit input admittance matrix," to $\mathbf{Y}_R$ as the "short-circuit reverse transfer admittance matrix," to $\mathbf{Y}_T$ as the "short-circuit forward transfer admittance matrix," and to $\mathbf{Y}_O$ as the "short-circuit output admittance matrix."

These matrices may also be simply referred to as the "input admittance matrix," the "reverse transfer admittance matrix," the "transfer admittance matrix," and the "output admittance matrix," respectively, when no confusion may occur. They have complex components and may be frequency dependent.

III. Design Equations

At a given frequency, the small-signal behavior of the ASC j may be described by the matrix $\mathbf{Y}_{\mathrm{A}j}$ defined by

$$\begin{pmatrix} i_{\mathrm{IA}j} \\ i_{\mathrm{CA}j} \\ i_{\mathrm{OA}j} \end{pmatrix} = \mathbf{Y}_{\mathrm{A}j} \begin{pmatrix} e_j \\ w_j \\ v_j \end{pmatrix} \tag{3}$$

in which (4) at the bottom of the page applies, where $y_{\mathrm{CTA}j}$ is the common terminal forward transfer admittance, $y_{\mathrm{OTA}j}$ is the output terminal forward transfer admittance, $y_{\mathrm{IA}j}$ is the input admittance, $y_{\mathrm{CMIA}j}$ is the common-mode input terminal admittance, $y_{\mathrm{IRA}j}$ is the input terminal reverse transfer admittance, $y_{\mathrm{CMCA}j}$ is the common-mode common terminal admittance, $y_{\mathrm{CRA}j}$ is the common terminal reverse transfer admittance, $y_{\mathrm{CMOA}j}$ is the common-mode output terminal admittance, and $y_{\mathrm{OA}j}$ is the output admittance of the ASC.

We have said in Section II that the ASC may have additional connections to the reference terminal and/or to one or more power supplies. At least one such connection is necessarily present when the sum of the first row-vector and third row-vector of the matrix $\mathbf{Y}_{\mathrm{A}j}$ is not equal to its second row-vector. Consequently, $\mathbf{Y}_{\mathrm{A}j}$ is generally not the indefinite admittance matrix of the ASC. When an ASC j has only three terminals, we note:

- that $i_{\mathrm{CA}j}$ is the sum of $i_{\mathrm{IA}j}$ and $i_{\mathrm{OA}j}$;
- that voltages applied simultaneously to the three terminals have no effect on the currents, i.e., $y_{\mathrm{CMIA}j} = y_{\mathrm{CMCA}j} = y_{\mathrm{CMOA}j} = 0$;
- that, at a given frequency, the small-signal behavior of the ASC j may be described by the admittance matrix $\mathbf{Y}_{TPj}$ of the two-port with respect to the sub-circuit common terminal, defined by

$$\begin{pmatrix} i_{\mathrm{IA}j} \\ i_{\mathrm{OA}j} \end{pmatrix} = \mathbf{Y}_{TPj} \begin{pmatrix} e_j - w_j \\ v_j - w_j \end{pmatrix} \tag{5}$$

where

$$\mathbf{Y}_{TPj} = \begin{pmatrix} y_{TP11j} & y_{TP12j} \\ y_{TP21j} & y_{TP22j} \end{pmatrix}. \tag{6}$$

Consequently, we have (7), shown at the bottom of the page, and the following equation :

$$\begin{cases} y_{\mathrm{IA}j} = y_{TP11j} \\ y_{\mathrm{IRA}j} = y_{TP12j} \\ y_{\mathrm{OA}j} = y_{TP22j} \\ y_{\mathrm{OTA}j} = y_{TP21j} \end{cases} \quad \begin{cases} y_{\mathrm{CTA}j} = y_{TP11j} + y_{TP21j} \\ y_{\mathrm{CMIA}j} = y_{\mathrm{CMCA}j} = y_{\mathrm{CMOA}j} = 0 \\ y_{\mathrm{CRA}j} = y_{TP12j} + y_{TP22j} \end{cases} \tag{8}$$

In order to provide simpler formulas for $\mathbf{Y}_T$ and $\mathbf{Y}_O$, we will from now on assume that all ASCs have substantially identical properties. Dropping the j indexes and using $\mathbf{1}_n$ to denote the identity matrix of size $n \times n$, we obtain the following general expressions, for any ASC described by (4):

$$\begin{aligned} \mathbf{Y}_I = {} & [(y_{\mathrm{IA}} + y_{\mathrm{CMIA}})\mathbf{1}_n + \{y_{\mathrm{IA}}(y_{\mathrm{CRA}} + 2y_{\mathrm{CMCA}}) \\ & + y_{\mathrm{CMIA}}(y_{\mathrm{CRA}} + 2y_{\mathrm{CTA}}) \\ & + y_{\mathrm{IRA}}(y_{\mathrm{CMCA}} - y_{\mathrm{CTA}})\}\mathbf{Z}_{\mathrm{FB}}] \\ & \times [\mathbf{1}_n + (y_{\mathrm{CTA}} + y_{\mathrm{CRA}} + y_{\mathrm{CMCA}})\mathbf{Z}_{\mathrm{FB}}]^{-1} \end{aligned} \tag{9}$$

$$\begin{aligned} \mathbf{Y}_R = {} & [(y_{\mathrm{IRA}} + y_{\mathrm{CMIA}})\mathbf{1}_n + \{y_{\mathrm{IRA}}(y_{\mathrm{CTA}} + 2y_{\mathrm{CMCA}}) \\ & + y_{\mathrm{CMIA}}(y_{\mathrm{CTA}} + 2y_{\mathrm{CRA}}) \\ & + y_{\mathrm{IA}}(y_{\mathrm{CMCA}} - y_{\mathrm{CRA}})\}\mathbf{Z}_{\mathrm{FB}}] \\ & \times [\mathbf{1}_n + (y_{\mathrm{CTA}} + y_{\mathrm{CRA}} + y_{\mathrm{CMCA}})\mathbf{Z}_{\mathrm{FB}}]^{-1} \end{aligned} \tag{10}$$

$$\mathbf{Y}_{\mathrm{A}j} = \begin{pmatrix} y_{\mathrm{IA}j} + y_{\mathrm{CMIA}j} & y_{\mathrm{CMIA}j} - y_{\mathrm{IA}j} - y_{\mathrm{IRA}j} & y_{\mathrm{IRA}j} + y_{\mathrm{CMIA}j} \\ y_{\mathrm{CTA}j} - y_{\mathrm{CMCA}j} & -y_{\mathrm{CTA}j} - y_{\mathrm{CRA}j} - y_{\mathrm{CMCA}j} & y_{\mathrm{CRA}j} - y_{\mathrm{CMCA}j} \\ y_{\mathrm{OTA}j} + y_{\mathrm{CMOA}j} & y_{\mathrm{CMOA}j} - y_{\mathrm{OTA}j} - y_{\mathrm{OA}j} & y_{\mathrm{OA}j} + y_{\mathrm{CMOA}j} \end{pmatrix} \tag{4}$$

$$\mathbf{Y}_{\mathrm{A}j} = \begin{pmatrix} y_{TP11j} & -y_{TP11j} - y_{TP12j} & y_{TP12j} \\ y_{TP11j} + y_{TP21j} & -y_{TP11j} - y_{TP12j} - y_{TP21j} - y_{TP22j} & y_{TP12j} + y_{TP22j} \\ y_{TP21j} & -y_{TP21j} - y_{TP22j} & y_{TP22j} \end{pmatrix} \tag{7}$$

$$\begin{aligned}\mathbf{Y}_T = &[(y_{\mathrm{OTA}} + y_{\mathrm{CMOA}})\mathbf{1}_n + \{y_{\mathrm{OTA}}(y_{\mathrm{CRA}} + 2y_{\mathrm{CMCA}}) \\ &+ y_{\mathrm{CMOA}}(y_{\mathrm{CRA}} + 2y_{\mathrm{CTA}}) \\ &+ y_{\mathrm{OA}}(y_{\mathrm{CMCA}} - y_{\mathrm{CTA}})\}\mathbf{Z}_{\mathrm{FB}}] \\ &\times [\mathbf{1}_n + (y_{\mathrm{CTA}} + y_{\mathrm{CRA}} + y_{\mathrm{CMCA}})\mathbf{Z}_{\mathrm{FB}}]^{-1} \end{aligned} \tag{11}$$

and

$$\begin{aligned}\mathbf{Y}_O = &[(y_{\mathrm{OA}} + y_{\mathrm{CMOA}})\mathbf{1}_n + \{y_{\mathrm{OA}}(y_{\mathrm{CTA}} + 2y_{\mathrm{CMCA}}) \\ &+ y_{\mathrm{CMOA}}(y_{\mathrm{CTA}} + 2y_{\mathrm{CRA}}) \\ &+ y_{\mathrm{OTA}}(y_{\mathrm{CMCA}} - y_{\mathrm{CRA}})\}\mathbf{Z}_{\mathrm{FB}}] \\ &\times [\mathbf{1}_n + (y_{\mathrm{CTA}} + y_{\mathrm{CRA}} + y_{\mathrm{CMCA}})\mathbf{Z}_{\mathrm{FB}}]^{-1}. \end{aligned} \tag{12}$$

For ASC having exactly three terminals, using (8), we get

$$\begin{aligned}\mathbf{Y}_I = &[y_{TP11}\mathbf{1}_n + \{y_{TP11}y_{TP22} - y_{TP12}y_{TP21}\}\mathbf{Z}_{\mathrm{FB}}] \\ &\times [\mathbf{1}_n + (y_{TP11} + y_{TP12} + y_{TP21} + y_{TP22})\,\mathbf{Z}_{\mathrm{FB}}]^{-1} \end{aligned} \tag{13}$$

$$\begin{aligned}\mathbf{Y}_R = &[y_{TP12}\mathbf{1}_n - \{y_{TP11}y_{TP22} - y_{TP12}y_{TP21}\}\mathbf{Z}_{\mathrm{FB}}] \\ &\times [\mathbf{1}_n + (y_{TP11} + y_{TP12} + y_{TP21} + y_{TP22})\,\mathbf{Z}_{\mathrm{FB}}]^{-1} \end{aligned} \tag{14}$$

$$\begin{aligned}\mathbf{Y}_T = &[y_{TP21}\mathbf{1}_n - \{y_{TP22}y_{TP11} - y_{TP12}y_{TP21}\}\mathbf{Z}_{\mathrm{FB}}] \\ &\times [\mathbf{1}_n + (y_{TP11} + y_{TP12} + y_{TP21} + y_{TP22})\,\mathbf{Z}_{\mathrm{FB}}]^{-1} \end{aligned} \tag{15}$$

and

$$\begin{aligned}\mathbf{Y}_O = &[y_{TP22}\mathbf{1}_n + \{y_{TP11}y_{TP22} - y_{TP12}y_{TP21}\}\,\mathbf{Z}_{\mathrm{FB}}] \\ &\times [\mathbf{1}_n + (y_{TP11} + y_{TP12} + y_{TP21} + y_{TP22})\,\mathbf{Z}_{\mathrm{FB}}]^{-1}\,. \end{aligned} \tag{16}$$

Using (11) or possibly (15), it is possible to proportion the ASC and $\mathbf{Z}_{\mathrm{FB}}$ in such a way that the negative feedback produces a $\mathbf{Y}_T$ which approximates a given matrix $\mathbf{Y}_G$. For instance, if we use ideal second-generation current conveyor (CCII) [1, ch. 58] for the ASC, we can assume that $|y_{\mathrm{CTA}}|$ is very large, that $y_{\mathrm{IA}} = y_{\mathrm{CMIA}} = y_{\mathrm{IRA}} = y_{\mathrm{CMCA}} = y_{\mathrm{CRA}} = y_{\mathrm{CMOA}} = y_{\mathrm{OA}} = 0$, and that $y_{\mathrm{OTA}} = \pm y_{\mathrm{CTA}}$. The case $y_{\mathrm{OTA}} = y_{\mathrm{CTA}}$ corresponds to a CCII-, and the case $y_{\mathrm{OTA}j} = -y_{\mathrm{CTA}j}$ to a CCII+. Using (9)–(12), we get

$$\mathbf{Y}_T \approx \pm\mathbf{Z}_{\mathrm{FB}}^{-1} \tag{17}$$

and

$$\mathbf{Y}_I = \mathbf{0}_n \quad \mathbf{Y}_R = \mathbf{0}_n \quad \mathbf{Y}_O = \mathbf{0}_n \tag{18}$$

where $\mathbf{0}_n$ is the null matrix of size $n \times n$. In (17), the positive sign applies if the ASCs are ideal CCII- and the negative sign if the ASCs are ideal CCII+.

At frequencies above ~ 100 MHz, using nearly ideal circuits like the CCII is not possible. However, an ASC can be made of a single transistor capable of multi-gigahertz operation. With a suitable biasing such an ASC will be adequate for unipolar operation.

IV. Example of Application

In this section, we present the design of a small-signal MIMO-SSFA, in which each ASC is made of a single bipolar transistor. The MIMO-SSFA is used as a transmitting circuit in the interconnection scheme shown in Fig. 3, in which the special ZXtalk method for completely degenerate interconnections [2] [7, § IX] is implemented with a matched termination at both ends. Such a scheme is applicable to simultaneous bi-directional signaling with reduced echo and crosstalk.

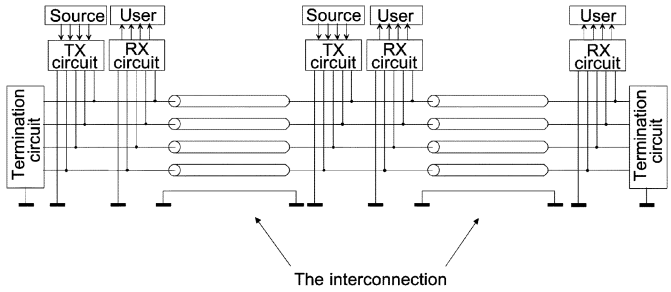

Fig. 3. Implementation of the special ZXtalk method for completely degenerate interconnections.

In Fig. 3, the transmitting circuits (TX circuits) are connected in parallel with the conductors of the interconnection. Since its input is driven by $n = 4$ independent low-impedance sources, a transmitting circuit is defined by the 2 following requirements.

- Each component of $\mathbf{Y}_O$ should have a small absolute value compared to absolute values of each component of the inverse of the characteristic impedance matrix $\mathbf{Z}_C$ of the interconnection, so that all voltage reflection coefficients caused by the transmitting circuit have a small absolute value.
- If $\mathbf{I}_T$ is the column-vector of the current injected by the output terminals of the transmitting circuit, we should have [7, eq. 21]:

$$\mathbf{I}_T = 2\mathbf{Z}_C^{-1}\mathrm{diag}_n\,(\alpha_1, \ldots, \alpha_n)\,\mathbf{X}_I \tag{19}$$

where $\mathrm{diag}_n(\alpha_1, \ldots, \alpha_n)$ is a diagonal matrix of nonzero proportionality coefficients α_i and where $\mathbf{X}_I$ is the column-vector of the n input voltages $x_{I1}, \ldots, x_{In}$ of the transmitting circuit.

In the example considered in [2], we have

$$\mathbf{Z}_C \approx \begin{pmatrix} 68.803 & 24.149 & 10.199 & 4.510 \\ 24.149 & 67.403 & 23.685 & 10.199 \\ 10.199 & 23.685 & 67.403 & 24.149 \\ 4.510 & 10.199 & 24.149 & 68.803 \end{pmatrix} \Omega. \tag{20}$$

Optimization parameters are needed for the design of a MIMO-SSFA meeting the above requirements. In Fig. 3, the matrix $\mathbf{P}_O$ of the voltage reflection coefficients [7, eq. 11], caused by the transmitting circuit, and the matrix $\mathbf{G}_V$ of the voltage gain for the nominal load impedance matrix $\mathbf{Z}_C/2$ are

$$\mathbf{P}_O = -\frac{1}{2}\mathbf{Z}_C\mathbf{Y}_O\left(\mathbf{1}_n + \frac{1}{2}\mathbf{Z}_C\mathbf{Y}_O\right)^{-1} \tag{21}$$

$$\mathbf{G}_V = -\left(\mathbf{1}_n + \frac{1}{2}\mathbf{Z}_C\mathbf{Y}_O\right)^{-1}\frac{1}{2}\mathbf{Z}_C\mathbf{Y}_T. \tag{22}$$

If our design was ideal, $\mathbf{P}_O$ would be near $\mathbf{0}_n$ and $\mathbf{G}_V$ would be a diagonal matrix. For the design of the MIMO-SSFA, our design target is a transfer admittance matrix $\mathbf{Y}_T$ approximating

$$\mathbf{Y}_G = (7\mathbf{Z}_C)^{-1} \tag{23}$$

and the minimization of two figures of merit: FMY is the figure of merit for the output admittance, defined as the maximum absolute row sum norm of $\mathbf{P}_O$, and FMG is the figure of merit for the voltage gain, defined as the maximum absolute row sum norm of the matrix obtained by subtracting $\mathbf{1}_n$ from the matrix resulting from the normalization of each row of $\mathbf{G}_V$ in such a way that the diagonal components are equal to 1. Note that $\mathrm{FMY} = 0$ for $\mathbf{Y}_O = 0$ and $\mathrm{FMG} = 0$ if and only if $\mathbf{G}_V$ is diagonal. Equation (23) complies with (19) for $\mathrm{diag}_n(\alpha_1, \ldots, \alpha_n) \approx 0.0714 \times \mathbf{1}_n$ and the corresponding gain given by (22) is $\mathbf{G}_V \approx -0.0714 \times \mathbf{1}_n$. Such a low gain is adequate for low-voltage signaling.

Our design is based on the y-parameters derived from s-parameters measured at $I_C = 10$ mA on 3 μm$\times$ 50 μm NPN transistors obtained with the bipolar UHF-1 process of Intersil [8], exhibiting a f_T of 8 GHz. In the frequency range of interest for our simulations (up to 3 GHz) we considered that such parameters are more dependable than the SPICE models available for these transistors. The design of the MIMO-SSFA consisted in the selection of an appropriate scaling of the cross-sectional area of the transistors, and the computation of an appropriate real impedance matrix $\mathbf{Z}_{\mathrm{FB}}$. We arbitrarily selected a frequency (100 MHz) for which we computed the real part of $\mathbf{Z}_{\mathrm{FB}}$ (since we wanted a FN merely made of resistors) using (15), (20) and (23), for different values of cross-sectional area of the transistors. After this synthesis step, FMY and FMG were plotted as a function of frequency, using (15), (16), (20)–(22). Good results were obtained with a reduction of cross-sectional area of the transistors by a factor of 10, and with

$$\mathbf{Z}_{\mathrm{FB}} = \begin{pmatrix} 418.69 & 165.96 & 70.06 & 30.97 \\ 165.96 & 409.05 & 162.76 & 70.06 \\ 70.06 & 162.76 & 409.05 & 165.96 \\ 30.97 & 70.06 & 165.96 & 418.69 \end{pmatrix} \Omega. \quad (24)$$

This impedance matrix can be realized using 10 resistors. Fig. 4 shows the corresponding MIMO-SSFA. The figures of merit are shown in Fig. 5, in the frequency range 100 MHz to 3 GHz. The performances of this transmitting circuit have been investigated [2] and it was shown that, compared to conventional single-ended transmission, the near-end crosstalk is effectively reduced in the whole frequency range, and the far-end crosstalk is significantly reduced up to 1.5 GHz, corresponding to about $f_T/5$. This result was obtained with very inexpensive means.

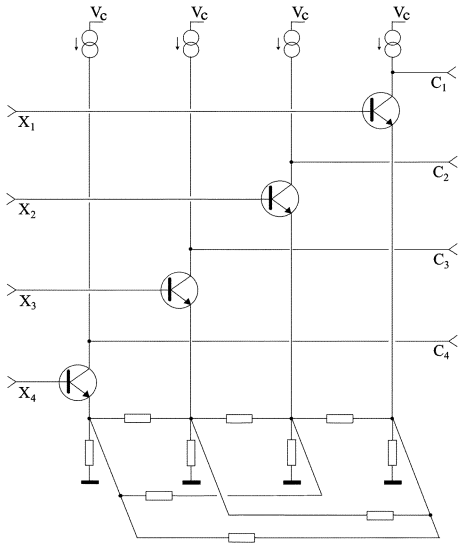

Fig. 4. MIMO SSFA used as a transmitting circuit.

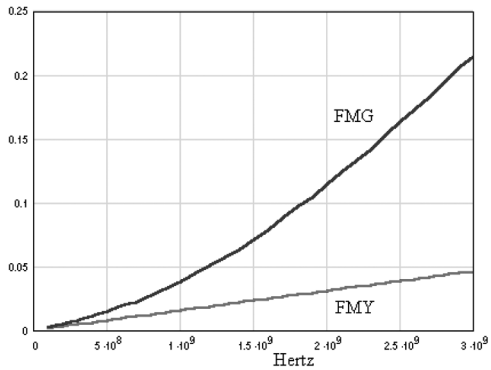

Fig. 5. Figures of merit FMY and FMG of the MIMO-SSFA (these figures of merit are zero for an ideal transmitting circuit).

V. Tailored Output Admittance Matrix

We have shown that it is possible to design a MIMO-SSFA providing a transfer admittance matrix $\mathbf{Y}_T$ approximating a given matrix $\mathbf{Y}_G$, for instance the one given by (20) and (23). We will now show that a MIMO-SSFA can use ASCs comprising an internal feedback loop, so as to obtain that the output impedance matrix $\mathbf{Y}_O$ approximates a wanted matrix $\mathbf{Y}_W$ such that

$$\mathbf{Y}_G = \zeta \mathbf{Y}_W \quad (25)$$

where ζ is a dimensionless scalar. The reason for such a requirement is the following. If the MIMO-SSFA designed in Section IV is used as a transmitting circuit installed at an end of the interconnection as shown on the left of Fig. 3, two networks of resistors are placed close to each other: the termination circuits having an impedance matrix approximating $\mathbf{Z}_C$ and the FN of the MIMO-SSFA. An output impedance matrix $\mathbf{Y}_O$ tailored according to (25) may be such that

$$\begin{cases} \mathbf{Y}_T \approx \zeta \mathbf{Z}_C^{-1} \\ \mathbf{Y}_O \approx \mathbf{Z}_C^{-1} \end{cases} \quad (26)$$

and, in this case, the MIMO-SSFA combines the functions of a transmitting circuit and of a termination circuit, thereby eliminating the need for the latter.

When no load is connected to the output (open-circuit), (26) implies that $\mathbf{V}_O = \zeta \mathbf{V}_I$. A first ASC structure capable of satisfying (26) is shown in Fig. 6. It comprises a voltage-controlled current source G1 of transconductance g, a voltage amplifier E1 of voltage gain K having a very large input impedance and a very small output impedance, and two resistors. We require $gK > 0$, so that E1 produces a negative feedback.

The internal feedback produces

$$\mathbf{Y}_{\mathrm{A}j} = \frac{1}{R_1 + R_2} \begin{pmatrix} 1 & 0 & -K \\ gR_2 & -g(KR_1 + R_2) & gKR_1 \\ gR_2 & -g(KR_1 + R_2) & gKR_1 \end{pmatrix} \quad (27)$$

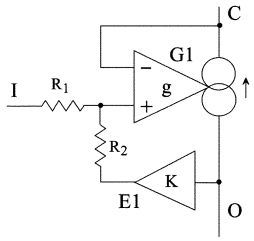

Fig. 6. First ASC structure compatible with (26).

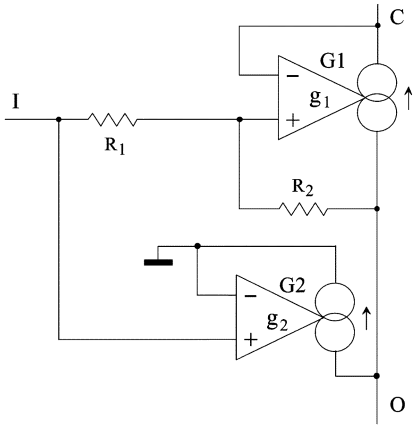

Fig. 7. Second ASC structure compatible with (26).

In the special case of n identical ASCs, using (11), (12) and (27), we obtain

$$\mathbf{Y}_T = \frac{gR_2}{R_1+R_2}\left[\mathbf{1}_n + g\frac{KR_1+R_2}{R_1+R_2}\mathbf{Z}_{\rm FB}\right]^{-1} \tag{28}$$

and

$$\mathbf{Y}_O = \frac{gKR_1}{R_1+R_2}\left[\mathbf{1}_n + g\frac{KR_1+R_2}{R_1+R_2}\mathbf{Z}_{\rm FB}\right]^{-1}. \tag{29}$$

This result is compatible with (26), for $\zeta = R_2/KR_1$. The voltage-controlled current source G1 could be replaced with a CCII- or with a CCII+, if an appropriate voltage gain K is used (for instance $K = +1$ for a CCII-, or $K = -1$ for a CCII+) to obtain a negative feedback and stability. However, in the shunt-shunt feedback loop shown in Fig. 6, having two active components connected in cascade adversely affects the achievable bandwidth of an actual implementation.

This difficulty is not present in a second ASC structure capable of satisfying (26), shown in Fig. 7. It comprises two voltage-controlled current sources G1 and G2 of transconductance g_1 and g_2, respectively, and two resistors. The internal feedback produces (30), shown at the bottom of the page.

For n identical ASCs, using (11), (12), and (30), we obtain

$$\mathbf{Y}_T = \left[\left(\frac{g_1R_2-1}{R_1+R_2}+g_2\right)\mathbf{1}_n + g_1\left(g_2 - \frac{1}{R_1+R_2}\right)\mathbf{Z}_{\rm FB}\right] \times \left[\mathbf{1}_n + g_1\mathbf{Z}_{\rm FB}\right]^{-1} \tag{31}$$

and

$$\mathbf{Y}_O = \left[\frac{g_1R_1+1}{R_1+R_2}\mathbf{1}_n + \frac{g_1}{R_1+R_2}\mathbf{Z}_{\rm FB}\right]\left[\mathbf{1}_n + g_1\mathbf{Z}_{\rm FB}\right]^{-1}. \tag{32}$$

If we choose $g_2 = 1/R_1$, this result is compatible with (26), for $\zeta = R_2/R_1$. The structure shown in Fig. 7 looks more appropriate for wideband implementations than the structure shown in Fig. 6, but this advantage is obtained at the cost of having to match g_2 and $1/R_1$. The voltage-controlled current sources G1 and G2 of Fig. 7 could both be replaced with a CCII-.

VI. Conclusion

The MIMO-SSFA is an interesting building block when a wideband circuit performing linear combinations between n input signals and n output signals is needed. This brief shows how the parameters of the FN and of the ASC may be used to obtain the desired characteristics, when a MIMO-SSFA is used as a transmitting circuit implementing the ZXtalk methods for the reduction of crosstalk and echo in electrical interconnections.

For such applications, device noise is often not important. However, for other possible applications of the MIMO-SSFA such as the RF front-end of radio receivers, a theoretical development for the assessment of noise would be necessary.

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$$\mathbf{Y}_{\mathrm{A}j} = \frac{1}{R_1+R_2}\begin{pmatrix} 1 & 0 & -1 \\ g_1R_2 & -g_1(R_1+R_2) & g_1R_1 \\ g_1R_2 - 1 + g_2(R_1+R_2) & -g_1(R_1+R_2) & g_1R_1+1 \end{pmatrix} \tag{30}$$