(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 December 2011 (29.12.2011)

PCT

(10) International Publication Number
WO 2011/161563 A1

(51) International Patent Classification:
H03F 3/45 (2006.01)

(21) International Application Number:
PCT/IB2011/052213

(22) International Filing Date:
20 May 2011 (20.05.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
1002662 25 June 2010 (25.06.2010) FR

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

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(54) Title: BALANCED-INPUT CURRENT-SENSING DIFFERENTIAL AMPLIFIER

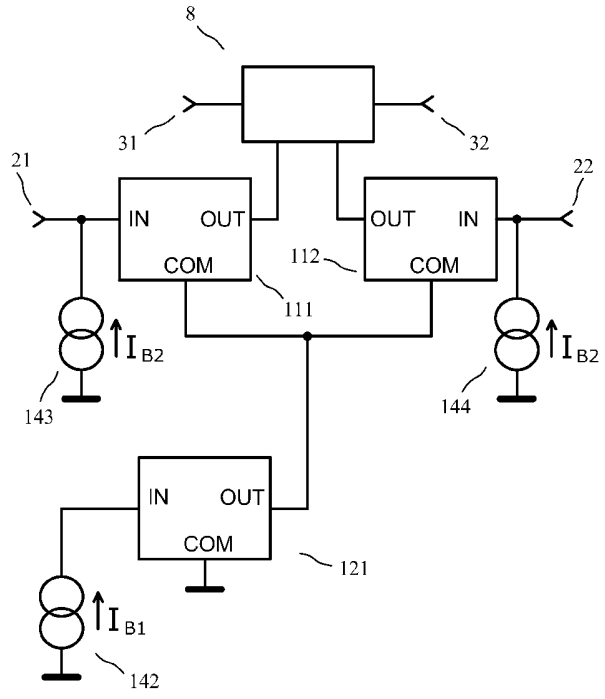


FIG. 9

(57) Abstract: The invention relates to a current-sensing differential amplifier having a balanced input. A balanced-input current-sensing differential amplifier of the invention has a first signal input terminal (21), a second signal input terminal (22), a first signal output terminal (31) and a second signal output terminal (32). The balanced-input current-sensing differential amplifier comprises a first current mirror (111), the input terminal of said first current mirror (111) being coupled to said first signal input terminal (21), a second current mirror (112), the input terminal of said second current mirror (112) being coupled to said second signal input terminal (22), a third current mirror (121), one of the output terminals of said third current mirror (121) being coupled to the common terminal of said first current mirror (111) and to the common terminal of said second current mirror (112), three current sources (142) (143) (144) and an output circuit (8).

WO 2011/161563 A1

SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

Balanced-input current-sensing differential amplifier

FIELD OF THE INVENTION

The invention relates to a current-sensing differential amplifier having a balanced input, such current-sensing differential amplifiers being for instance used as the input circuit of differential line receivers for electrical links used for transmitting analog or digital signals.

The French patent application number 10/02662 of 25 June 2010, entitled "Amplificateur différentiel captant le courant à entrée équilibrée" is incorporated by reference.

PRIOR ART

A differential amplifier has two signal input terminals. An output variable (voltage or current) of a current-sensing differential amplifier is mainly determined by the difference of the currents flowing into said signal input terminals, or equivalently by the differential-mode input current flowing through the signal input terminals, denoted by i_{DM}. A differential amplifier has a balanced input if and only if the behavior of the input is substantially invariant when the signal input terminals are permuted. For small signals, the input admittance matrix, with respect to ground, of a differential amplifier, denoted by $\mathbf{Y}_I$, is a 2×2 matrix. In the case of a balanced-input differential amplifier, $\mathbf{Y}_I$ is invariant when the signal input terminals are permuted, so that $\mathbf{Y}_I$ is given by

$$\mathbf{Y}_I = \begin{pmatrix} y_{I11} & y_{I12} \\ y_{I12} & y_{I11} \end{pmatrix} \tag{1}$$

If a differential-mode input voltage, denoted by v_{DM}, is applied to the signal input terminals, the differential-mode input current i_{DM} flowing through the signal input terminals is such that

$$\begin{pmatrix} i_{DM} \\ -i_{DM} \end{pmatrix} = \begin{pmatrix} y_{I11} & y_{I12} \\ y_{I12} & y_{I11} \end{pmatrix} \begin{pmatrix} v_{DM}/2 \\ -v_{DM}/2 \end{pmatrix} \tag{2}$$

Thus, the differential-mode input impedance, denoted by z_{DM}, is given by

$$z_{DM} = \frac{v_{DM}}{i_{DM}} = \frac{2}{y_{I11} - y_{I12}} \tag{3}$$

If a common-mode input voltage, denoted by v_{CM}, is applied to the signal input terminals, the common-mode input current i_{CM} flowing into the signal input terminals is such that

$$\begin{pmatrix} i_{CM}/2 \\ i_{CM}/2 \end{pmatrix} = \begin{pmatrix} y_{I11} & y_{I12} \\ y_{I12} & y_{I11} \end{pmatrix} \begin{pmatrix} v_{CM} \\ v_{CM} \end{pmatrix} \tag{4}$$

Thus, the common-mode input admittance, denoted by y_{CM}, is given by

$$y_{CM} = \frac{i_{CM}}{v_{CM}} = 2\left(y_{I11} + y_{I12}\right) \quad (5)$$

In Fig. 1, a first example of balanced-input current-sensing differential amplifier (1) has two signal input terminals (21) (22) and one signal output terminal (31) for delivering a single-ended output signal. In Fig. 2, a second example of balanced-input current-sensing differential amplifier (1) has two signal input terminals (21) (22) and two signal output terminals (31) (32) for delivering a differential output signal. In Fig. 1 and Fig. 2, the ground terminal and the power supply terminal(s) of the balanced-input current-sensing differential amplifier are not shown.

In the article of L. Zhang, J. Wilson, R. Bashirullah and P. Franzon entitled "Differential Current-Mode Signaling for Robust and Power Efficient On-Chip Global Interconnects", published in the *Proceedings of the IEEE 14th Topical Meeting on Electrical Performance of Electronic Packaging, EPEP 2005*, October 2005, at the pages 315 to 318, a receiver for a differential current-mode signaling scheme uses "current mode sensing". In this receiver, a small voltage is built on a sense resistor, referred to as "bridge resistor", connected to the two signal input terminals. This voltage is sensed by a conventional voltage-sensing differential amplifier. Typically, line receivers for links using low-voltage differential signaling (LVDS) or current-mode logic (CML) comprise this type of balanced-input current-sensing differential amplifier, which presents a low differential-mode input impedance and a low common-mode input admittance.

In the context of high-speed links, this type of balanced-input current-sensing differential amplifier has two major shortcomings:

- the voltage-sensing differential amplifier must sense a small voltage across a resistor, so that a substantial noise is present at the output of this amplifier;
- the "output variable versus differential-mode input current" characteristic is not well controlled because no global feedback can be used in the voltage-sensing differential amplifier, so that this characteristic depends on manufacturing process variations and on temperature, and has a poor linearity (for large signals).

In the differential current-mode input circuit presented in the article of M. Ishibe, S. Otaka, J. Takeda, S. Tanaka, Y. Toyoshima, S. Takatsuka and S. Shimizu entitled "High-Speed I/O Buffer Circuits", published in the *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 4, April 1992, at the pages 671 to 673, each signal input terminal is connected to the sources of complementary transistors each used in a common-gate configuration. This type of balanced-input current-sensing differential amplifier has a good linearity but it has the drawback of presenting a high common-mode input admittance, so that a common-mode current, which usually corresponds to disturbances caused by nearby circuits, can flow through the input.

Differential current-mode input circuits may also comprise current mirrors. In the present patent application, "current mirror" always refers to a current mirror comprising two or more

transistors of any type (bipolar transistor, field effect transistor, etc), providing an output current essentially proportional to the input current over a wide range of input current, and providing a low input impedance for small signals. Such current mirrors are explained in the chapters 2, 6, 7 and 8 of the book of C. Toumazou, F.J. Lidgey and D.G. Haigh entitled *Analog IC design: the current-mode approach*, published by Peter Peregrinus Ltd, in 1990. In the present patent application, "current mirror" always refers to a non-inverting current mirror in which the output current variation has the same orientation as the input current variation. The polarity of such a current mirror may be positive or negative. For instance, Fig. 3 shows a positive current mirror (4), having an input terminal (5), an output terminal (6) and a common terminal (7), in which a positive current, denoted by I, flows into the input terminal (5) and a positive current, equal to $k\,I$, flows into the output terminal (6), where k is a positive current gain. For instance, Fig. 4 shows a negative current mirror (4), having an input terminal (5), an output terminal (6) and a common terminal (7), in which a positive current, denoted by I, flows out of the input terminal (5) and a positive current, equal to $k\,I$, flows out of the output terminal (6), where k is a positive current gain. A current mirror may have several output terminals.

The Fig. 5 shows an example of a schematic diagram of a negative current mirror (4), having an input terminal (5), an output terminal (6) and a common terminal (7), comprising two PNP bipolar transistors (41) (42). The Fig. 6 shows an example of a schematic diagram of a positive current mirror (4), having an input terminal (5), an output terminal (6) and a common terminal (7), comprising three NPN bipolar transistors (43) (44) (45). The Fig. 7 shows an example of a schematic diagram of a negative current mirror (4), having an input terminal (5), an output terminal (6) and a common terminal (7), comprising two p-channel insulated gate field-effect transistors (MOSFETs) operating in the saturation regime (41) (42). The Fig. 8 shows an example of a schematic diagram of a positive current mirror (4), having an input terminal (5), an output terminal (6) and a common terminal (7), comprising two n-channel MOSFETs operating in the saturation regime (41) (42).

The differential current-mode input circuits shown in the figures 1 and 2 of the patent of the United States of America number 7,471,110, entitled "Current mode interface for off-chip high speed communication", use independent current mirror input stages for each signal input terminal. Like the previous type of input circuit, this type of balanced-input current-sensing differential amplifier has a good linearity but it has the drawback of presenting a high common-mode input admittance.

SUMMARY OF THE INVENTION

The purpose of the invention is a balanced-input current-sensing differential amplifier which overcomes the above-mentioned limitations of known techniques.

According to the invention, a balanced-input current-sensing differential amplifier

having a first signal input terminal and a second signal input terminal comprises:

a first current mirror having an input terminal, a common terminal and at least one output terminal, the input terminal of said first current mirror being coupled to said first signal input terminal, said first current mirror being of a given polarity;

a second current mirror having an input terminal, a common terminal and at least one output terminal, the input terminal of said second current mirror being coupled to said second signal input terminal, said second current mirror being of said given polarity;

a third current mirror having an input terminal, a common terminal and at least one output terminal, one of the output terminals of said third current mirror being coupled to the common terminal of said first current mirror and to the common terminal of said second current mirror, said third current mirror being of said given polarity.

We see that, according to the invention, the first current mirror, the second current mirror and the third current mirror have the same polarity, so that they are either all positive or all negative.

The balanced-input current-sensing differential amplifier of the invention may be such that the current flowing into the input terminal of said third current mirror is substantially independent from a voltage applied to said first signal input terminal and from a voltage applied to said second signal input terminal. For instance, the current flowing into the input terminal of said third current mirror may be a constant current.

A balanced-input current-sensing differential amplifier of the invention may further comprise:

a fourth current mirror having an input terminal, a common terminal and at least one output terminal, the input terminal of said fourth current mirror being coupled to said first signal input terminal, said fourth current mirror being of the polarity opposite to said given polarity;

a fifth current mirror having an input terminal, a common terminal and at least one output terminal, the input terminal of said fifth current mirror being coupled to said second signal input terminal, said fifth current mirror being of the polarity opposite to said given polarity;

a sixth current mirror having an input terminal, a common terminal and at least one output terminal, one of the output terminals of said sixth current mirror being coupled to the common terminal of said fourth current mirror and to the common terminal of said fifth current mirror, said sixth current mirror being of the polarity opposite to said given polarity.

We see that, according to the invention, if the first current mirror, the second current mirror and the third current mirror are positive current mirrors, then the fourth current mirror, the fifth current mirror and the sixth current mirror are negative current mirrors. We see that, conversely, if the first current mirror, the second current mirror and the third current mirror are

negative current mirrors, then the fourth current mirror, the fifth current mirror and the sixth current mirror are positive current mirrors.

Additionally, this balanced-input current-sensing differential amplifier of the invention may be such that the current flowing into the input terminal of said sixth current mirror is substantially independent from a voltage applied to said first signal input terminal and from a voltage applied to said second signal input terminal. For instance, the current flowing into the input terminal of said sixth current mirror may be a constant current.

BRIEF DESCRIPTION OF THE DRAWINGS

Other advantages and characteristics will appear more clearly from the following description of particular embodiments of the invention, given by way of non-limiting examples, with reference to the accompanying drawings in which:

- Figure 1 shows a first example of balanced-input current-sensing differential amplifier, and has already been discussed in the section dedicated to the presentation of prior art;
- Figure 2 shows a second example of balanced-input current-sensing differential amplifier, and has already been discussed in the section dedicated to the presentation of prior art;
- Figure 3 shows a positive current mirror, and has already been discussed in the section dedicated to the presentation of prior art;
- Figure 4 shows a negative current mirror, and has already been discussed in the section dedicated to the presentation of prior art;
- Figure 5 shows a schematic diagram of a negative current mirror, and has already been discussed in the section dedicated to the presentation of prior art;
- Figure 6 shows a schematic diagram of a positive current mirror, and has already been discussed in the section dedicated to the presentation of prior art;
- Figure 7 shows a schematic diagram of a negative current mirror, and has already been discussed in the section dedicated to the presentation of prior art;
- Figure 8 shows a schematic diagram of a positive current mirror, and has already been discussed in the section dedicated to the presentation of prior art;
- Figure 9 shows the block diagram of a first embodiment of the invention;
- Figure 10 shows the schematic diagram of a second embodiment of the invention;
- Figure 11 shows the block diagram of a third embodiment of the invention;
- Figure 12 shows the schematic diagram of a fourth embodiment of the invention.

DETAILED DESCRIPTION OF SOME EMBODIMENTS

First embodiment.

As a first embodiment of a device of the invention, given by way of non-limiting example, we have represented in Fig. 9 the block diagram of a balanced-input current-sensing differential amplifier of the invention, having a first signal input terminal (21), a second signal input terminal (22), a first signal output terminal (31) and a second signal output terminal (32), the balanced-input current-sensing differential amplifier comprising:

a first current mirror (111) of a given polarity, said first current mirror having an input terminal, a common terminal and at least one output terminal, the input terminal of said first current mirror (111) being coupled to said first signal input terminal (21);

a second current mirror (112) of said given polarity, said second current mirror having an input terminal, a common terminal and at least one output terminal, the input terminal of said second current mirror (112) being coupled to said second signal input terminal (22);

a third current mirror (121) of said given polarity, said third current mirror having an input terminal, a common terminal and at least one output terminal, one of the output terminals of said third current mirror (121) being coupled to the common terminal of said first current mirror (111) and to the common terminal of said second current mirror (112).

The common terminal of said third current mirror (121) is grounded. The current flowing into the input terminal of said third current mirror (121) is a constant current, denoted by I_{B1}, delivered by a current source (142), so that the current flowing into the input terminal of said third current mirror (121) is independent from a voltage applied to said first signal input terminal (21) and from a voltage applied to said second signal input terminal (22). The first current mirror (111) and the second current mirror (112) are substantially identical and have a positive current gain, denoted by k. The third current mirror (121) has a positive current gain, denoted by K. The input terminals of the first current mirror (111) and of the second current mirror (112) are biased by two current sources (143) (144) each providing a constant current I_{B2} such that

$$K I_{B1} \approx 2 (k + 1) I_{B2} \quad (6)$$

The specialist understands that the current sources shown in Fig. 9 and in the next figures are ideal circuit elements which may be realized with real components, for instance using current mirrors.

An output circuit (8) is connected to the output terminals of the first current mirror (111) and of the second current mirror (112) and to the signal output terminals (31) (32). The output circuit (8) is such that, in the intended frequency range of operation:

- the voltage delivered by the first signal output terminal (31) is substantially equal to the sum

of a constant voltage and of a first variable voltage proportional to the difference between the current flowing into the first signal input terminal (21) and the current flowing into the second signal input terminal (22);

- the voltage delivered by the second signal output terminal (32) is substantially equal to the sum of said constant voltage and of a second variable voltage equal to the opposite of said first variable voltage.

The power supply terminal(s) needed to power feed the balanced-input current-sensing differential amplifier is(are) not shown in Fig. 9.

Second embodiment (best mode).

As a second embodiment of a device of the invention, given by way of non-limiting example and best mode of carrying out the invention, we have represented in Fig. 10 the schematic diagram of a balanced-input current-sensing differential amplifier of the invention, having a first signal input terminal (21), a second signal input terminal (22), a first signal output terminal (31) and a second signal output terminal (32), the balanced-input current-sensing differential amplifier comprising:

a first positive current mirror consisting of two n-channel MOSFETs (1111) (1112), said first positive current mirror having an input terminal, a common terminal and an output terminal, the input terminal of said first positive current mirror being coupled to said first signal input terminal (21);

a second positive current mirror consisting of two n-channel MOSFETs (1121) (1122), said second positive current mirror having an input terminal, a common terminal and an output terminal, the input terminal of said second positive current mirror being coupled to said second signal input terminal (22);

a third positive current mirror consisting of four n-channel MOSFETs (1211) (1212) (1213) (1214), said third positive current mirror having an input terminal, a common terminal and three output terminals, one of the output terminals of said third positive current mirror being coupled to the common terminal of said first positive current mirror and to the common terminal of said second positive current mirror.

The common terminal of said third positive current mirror is grounded, the ground symbol used in Fig. 10 and in Fig. 12 having exactly the same meaning as the other ground symbol used in Fig. 9 and in Fig. 11. A voltage source (1411) power feeds the balanced-input current-sensing differential amplifier shown in Fig. 10. A current source (1412) delivers a constant current to the input of a negative current mirror having three output terminals, consisting of four p-channel MOSFETs (1413) (1421) (1431) (1441). This negative current mirror is used for biasing the input terminal of said first positive current mirror with a constant current I_{B2}, the input terminal of said second positive current mirror with the same constant

current I_{B2}, and the input terminal of said third positive current mirror with a constant current I_{B1}. The current flowing into the input terminal of said third positive current mirror is therefore substantially independent from a voltage applied to said first signal input terminal (21) and from a voltage applied to said second signal input terminal (22). The first positive current mirror and the second positive current mirror are substantially identical and have a positive current gain, denoted by k. The third positive current mirror has a positive current gain, denoted by K. The equation (6) is satisfied.

An output circuit comprises:

- a first output current mirror consisting of two p-channel MOSFETs (1311) (1312) and a peaking inductor (1313);
- a second output current mirror consisting of two p-channel MOSFETs (1321) (1322) and a peaking inductor (1323).

The specialist understands that the circuit elements shown in Fig. 10 may be proportioned such that, in the intended frequency range of operation:

- the current delivered by the first signal output terminal (31) is substantially proportional to the difference between the current flowing into the first signal input terminal (21) and the current flowing into the second signal input terminal (22);
- the current delivered by the second signal output terminal (32) is substantially the opposite of the current delivered by the first signal output terminal (31).

The balanced-input current-sensing differential amplifier shown in Fig. 10 provides a bandwidth of 5 GHz, it presents a low differential-mode input impedance, of about 430 Ω in the frequency range dc to 5 GHz, and it presents a low common-mode input admittance. This balanced-input current-sensing differential amplifier does not use a voltage-sensing differential amplifier for sensing a small voltage across a resistor. The specialist understands that the "output current versus differential-mode input current" characteristic of this balanced-input current-sensing differential amplifier is well controlled (it depends neither on manufacturing process variations nor on temperature) and has a good linearity. The specialist also understands that the "differential-mode input voltage versus differential-mode input current" characteristic of this balanced-input current-sensing differential amplifier has a good linearity, and may easily correspond to a differential-mode input impedance in the range 100 Ω to 2000 Ω.

Third embodiment.

As a third embodiment of a device of the invention, given by way of non-limiting example, we have represented in Fig. 11 the block diagram of a balanced-input current-sensing differential amplifier of the invention having a first signal input terminal (21), a second signal input terminal (22) and a signal output terminal (31), the balanced-input current-sensing differential amplifier comprising:

a first positive current mirror (111) having an input terminal, a common terminal and at least one output terminal, the input terminal of said first positive current mirror (111) being coupled to said first signal input terminal (21);

a second positive current mirror (112) having an input terminal, a common terminal and at least one output terminal, the input terminal of said second positive current mirror (112) being coupled to said second signal input terminal (22);

a third positive current mirror (121) having an input terminal, a common terminal and at least one output terminal, one of the output terminals of said third positive current mirror (121) being coupled to the common terminal of said first positive current mirror (111) and to the common terminal of said second positive current mirror (112);

a first negative current mirror (113) having an input terminal, a common terminal and at least one output terminal, the input terminal of said first negative current mirror (113) being coupled to said first signal input terminal (21);

a second negative current mirror (114) having an input terminal, a common terminal and at least one output terminal, the input terminal of said second negative current mirror (114) being coupled to said second signal input terminal (22);

a third negative current mirror (122) having an input terminal, a common terminal and at least one output terminal, one of the output terminals of said third negative current mirror (122) being coupled to the common terminal of said first negative current mirror (113) and to the common terminal of said second negative current mirror (114).

The common terminal of said third positive current mirror (121) is grounded. The common terminal of said third negative current mirror (122) is connected to a power supply node. The current flowing into the input terminal of said third positive current mirror (121) is delivered by a current source (142) providing a constant current I_{B1}, and the current flowing out of the input terminal of said third negative current mirror (122) is delivered by a current source (141) providing the same constant current I_{B1}. Thus, the current flowing into the input terminal of said third positive current mirror (121) and the current flowing out of the input terminal of said third negative current mirror (122) are independent from a voltage applied to said first signal input terminal (21) and from a voltage applied to said second signal input terminal (22). The first positive current mirror (111) and the second positive current mirror (112) are substantially identical and have a positive current gain, denoted by k. The first negative current mirror (113) and the second negative current mirror (114) are substantially identical and have a positive current gain substantially equal to k.

An output circuit (8) is connected to the output terminals of the first positive current mirror (111), of the second positive current mirror (112), of the first negative current mirror (113) and of the second negative current mirror (114), and to the signal output terminal (31). The output circuit (8) is such that, in the intended frequency range of operation, the voltage delivered by the signal output terminal (31) is substantially equal to the sum of a constant

voltage and of a variable voltage proportional to the difference between the current flowing into the first signal input terminal (21) and the current flowing into the second signal input terminal (22).

The power supply terminal(s) needed to power feed the output circuit (8) is (are) not shown in Fig. 11.

Fourth embodiment.

As a fourth embodiment of a device of the invention, given by way of non-limiting example, we have represented in Fig. 12 the schematic diagram of a balanced-input current-sensing differential amplifier of the invention having a first signal input terminal (21), a second signal input terminal (22), a first signal output terminal (31) and a second signal output terminal (32), the balanced-input current-sensing differential amplifier comprising:

a first positive current mirror consisting of two NPN bipolar transistors (1111) (1112), said first positive current mirror having an input terminal, a common terminal and an output terminal, the input terminal of said first positive current mirror being coupled to said first signal input terminal (21);

a second positive current mirror consisting of two NPN bipolar transistors (1121) (1122), said second positive current mirror having an input terminal, a common terminal and an output terminal, the input terminal of said second positive current mirror being coupled to said second signal input terminal (22);

a third positive current mirror consisting of two NPN bipolar transistors (1211) (1212), said third positive current mirror having an input terminal, a common terminal and an output terminal, the output terminal of said third positive current mirror being coupled to the common terminal of said first positive current mirror and to the common terminal of said second positive current mirror;

a first negative current mirror consisting of two PNP bipolar transistors (1131) (1132), said first negative current mirror having an input terminal, a common terminal and an output terminal, the input terminal of said first negative current mirror being coupled to said first signal input terminal (21);

a second negative current mirror consisting of two PNP bipolar transistors (1141) (1142), said second negative current mirror having an input terminal, a common terminal and an output terminal, the input terminal of said second negative current mirror being coupled to said second signal input terminal (22);

a third negative current mirror consisting of three PNP bipolar transistors (1221) (1421) (1222), said third negative current mirror having an input terminal, a common terminal and two output terminals, one of the output terminals of said third negative current mirror being coupled to the common terminal of said first negative current mirror and to the common

terminal of said second negative current mirror.

A voltage source (1411) power feeds the balanced-input current-sensing differential amplifier shown in Fig. 12. The common terminal of said third positive current mirror is grounded. The common terminal of said third negative current mirror is connected to a power supply node. A current source (1412) delivers a constant current to the input of said third negative current mirror. The third negative current mirror delivers a constant current to the input terminal of said third positive current mirror. Thus, the current flowing into the input terminal of said third positive current mirror and the current flowing out of the input terminal of said third negative current mirror are substantially independent from a voltage applied to said first signal input terminal (21) and from a voltage applied to said second signal input terminal (22). The first positive current mirror, the second positive current mirror, the first negative current mirror and the second negative current mirror have substantially the same current gain.

An output circuit comprises:

- a first output current mirror made of two PNP bipolar transistors (1311) (1312);
- a second output current mirror made of two PNP bipolar transistors (1321) (1322);
- a third output current mirror made of two NPN bipolar transistors (1331) (1332);
- a fourth output current mirror made of two NPN bipolar transistors (1341) (1342).

The specialist understands that the circuit elements shown in Fig. 12 may be proportioned such that, in the intended frequency range of operation:

- the current delivered by the first signal output terminal (31) is substantially proportional to the difference between the current flowing into the first signal input terminal (21) and the current flowing into the second signal input terminal (22);
- the current delivered by the second signal output terminal (32) is substantially the opposite of the current delivered by the first signal output terminal (31).

The balanced-input current-sensing differential amplifier shown in Fig. 12 provides a bandwidth of 10 GHz, it presents a low differential-mode input impedance, of about 50 Ω in the frequency range dc to 10 GHz, and it presents a low common-mode input admittance. This balanced-input current-sensing differential amplifier does not use a voltage-sensing differential amplifier for sensing a small voltage across a resistor. The specialist understands that the "output current versus differential-mode input current" characteristic of this balanced-input current-sensing differential amplifier is well controlled and has a good linearity. The specialist also understands that the "differential-mode input voltage versus differential-mode input current" characteristic of this balanced-input current-sensing differential amplifier has a good linearity, and may easily correspond to a differential-mode input impedance in the range 10 Ω to 250 Ω, which can be adjusted with the current delivered by the current source (1412). Thus, the differential-mode input impedance of a balanced-input current-sensing differential amplifier of the invention can be adjusted by electrical means.

INDICATIONS ON INDUSTRIAL APPLICATIONS

The specialist understands that a balanced-input current-sensing differential amplifier of the invention may be used as a part of a line receiver for differential electrical links used for transmitting analog or digital signals, typically as the input circuit of the line receiver for differential electrical links. In this case, the signal input terminals of the balanced-input current-sensing differential amplifier of the invention are coupled to the transmission conductors of the balanced interconnection.

In the context of high-speed links, the balanced-input current-sensing differential amplifier of the invention has the following advantages:

- it does not use a voltage-sensing differential amplifier for sensing a small voltage across a resistor;
- it presents a low common-mode input admittance;
- the "output variable versus differential-mode input current" characteristic is well controlled and may have a good linearity, this property being very important for high-performance multilevel digital signaling and for simultaneous bidirectional signaling;
- the "differential-mode input voltage versus differential-mode input current" characteristic has a good linearity and it may provide a differential-mode input impedance suitable for canceling reflections in a differential link, thereby eliminating the need for a termination;
- the differential-mode input impedance may be adjustable by electrical means.

CLAIMS

1. A balanced-input current-sensing differential amplifier having a first signal input terminal (21) and a second signal input terminal (22), the balanced-input current-sensing differential amplifier comprising:

a first current mirror (111) having an input terminal, a common terminal and at least one output terminal, the input terminal of said first current mirror (111) being coupled to said first signal input terminal (21), said first current mirror being of a given polarity;

a second current mirror (112) having an input terminal, a common terminal and at least one output terminal, the input terminal of said second current mirror (112) being coupled to said second signal input terminal (22), said second current mirror being of said given polarity;

a third current mirror (121) having an input terminal, a common terminal and at least one output terminal, one of the output terminals of said third current mirror (121) being coupled to the common terminal of said first current mirror (111) and to the common terminal of said second current mirror (112), said third current mirror (121) being of said given polarity.

2. The balanced-input current-sensing differential amplifier of claim 1, wherein the current flowing into the input terminal of said third current mirror (121) is substantially independent from a voltage applied to said first signal input terminal (21) and from a voltage applied to said second signal input terminal (22).

3. The balanced-input current-sensing differential amplifier of any of the claims 1 or 2, wherein the current flowing into the input terminal of said third current mirror (121) is a constant current.

4. The balanced-input current-sensing differential amplifier of any of the claims 1 to 3, wherein the first current mirror (111) and the second current mirror (112) are substantially identical.

5. The balanced-input current-sensing differential amplifier of any of the claims 1 to 4, further comprising:

a fourth current mirror (113) having an input terminal, a common terminal and at least one output terminal, the input terminal of said fourth current mirror (113) being coupled to said first signal input terminal (21), said fourth current mirror (113) being of the polarity opposite to said given polarity;

a fifth current mirror (114) having an input terminal, a common terminal and at least one output terminal, the input terminal of said fifth current mirror (114) being coupled to said second signal input terminal (22), said fifth current mirror (114) being of the polarity

opposite to said given polarity;

a sixth current mirror (122) having an input terminal, a common terminal and at least one output terminal, one of the output terminals of said sixth current mirror (122) being coupled to the common terminal of said fourth current mirror (113) and to the common terminal of said fifth current mirror (114), said sixth current mirror (122) being of the polarity opposite to said given polarity.

6. The balanced-input current-sensing differential amplifier of claim 5, wherein the current flowing into the input terminal of said sixth current mirror (122) is substantially independent from a voltage applied to said first signal input terminal (21) and from a voltage applied to said second signal input terminal (22).

7. The balanced-input current-sensing differential amplifier of any of the claims 5 or 6, wherein the current flowing into the input terminal of said sixth current mirror (122) is a constant current.

8. The balanced-input current-sensing differential amplifier of any of the claims 5 to 7, wherein the first current mirror (111) and the second current mirror (112) are substantially identical and have a positive current gain, denoted by k, and wherein the fourth current mirror (113) and the fifth current mirror (114) are substantially identical and have a positive current gain substantially equal to k.

9. The balanced-input current-sensing differential amplifier of any of the claims 1 to 8, wherein the differential-mode input impedance of the balanced-input current-sensing differential amplifier can be adjusted by electrical means.

10. The balanced-input current-sensing differential amplifier of any of the claims 1 to 9, wherein said balanced-input current-sensing differential amplifier constitutes a part of a line receiver for differential electrical links.

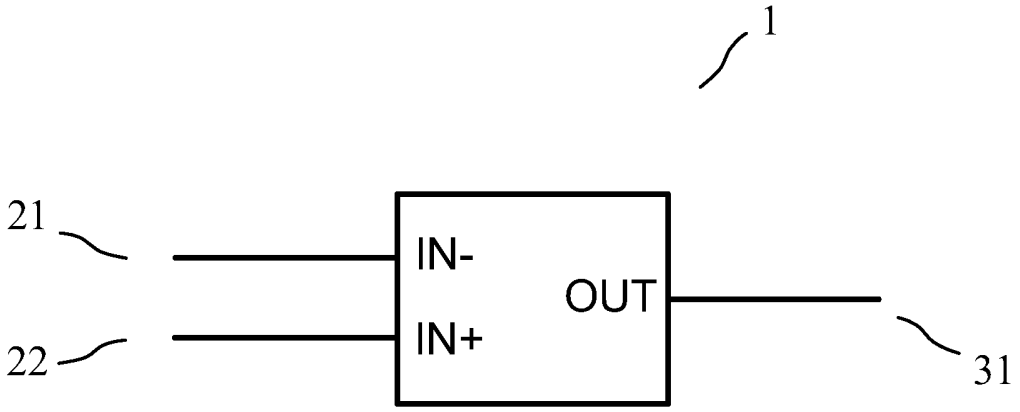


FIG. 1

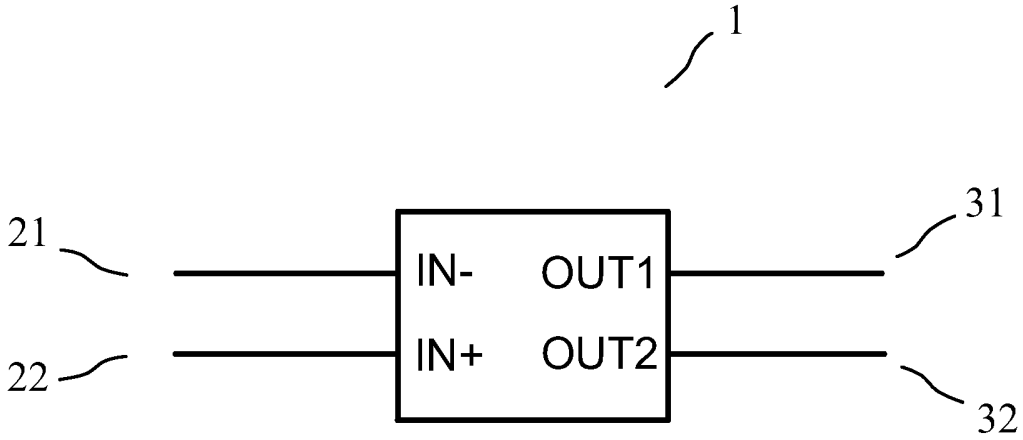


FIG. 2

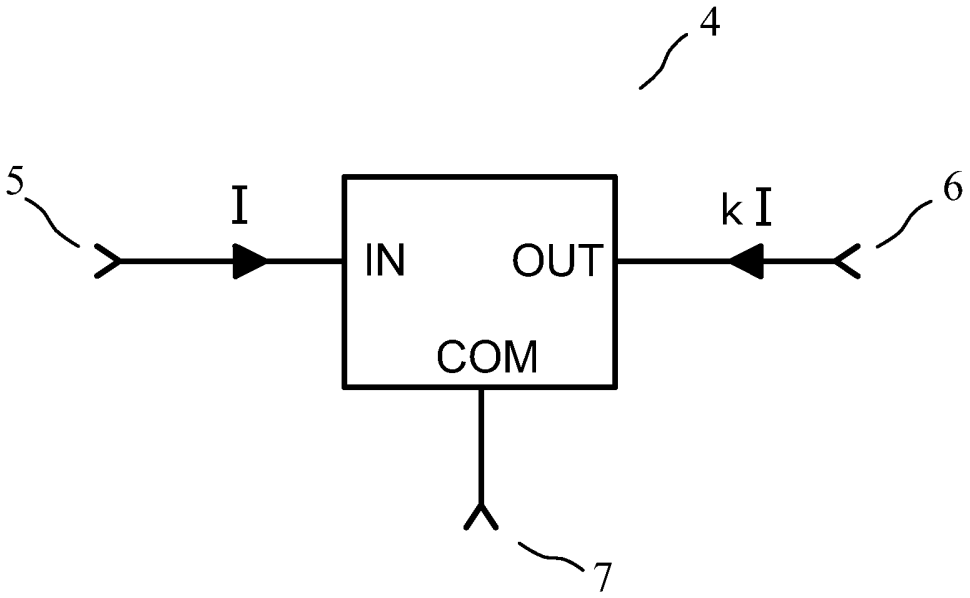


FIG. 3

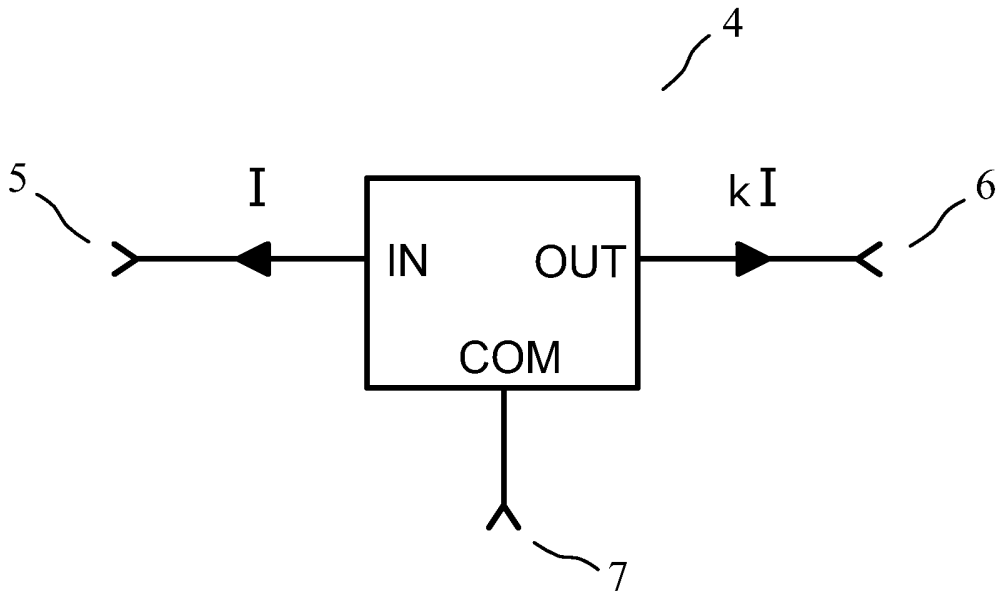


FIG. 4

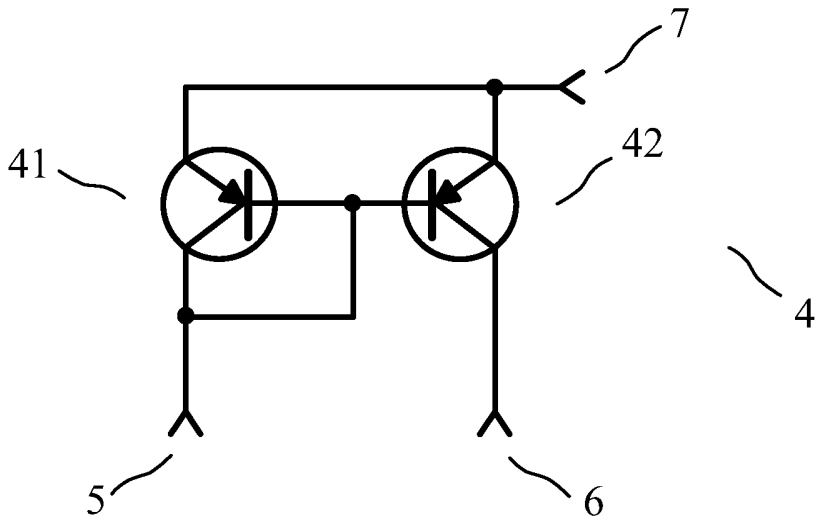


FIG. 5

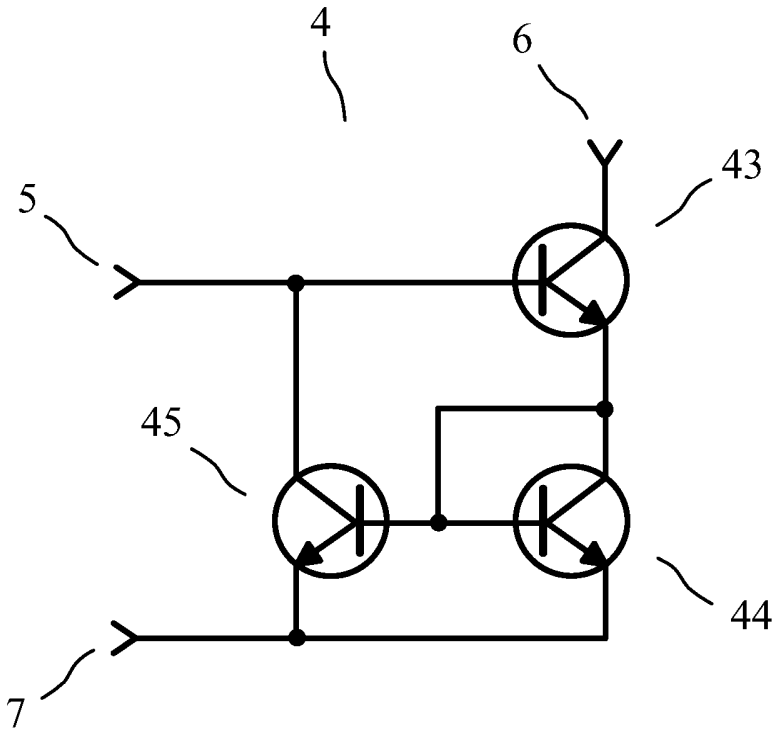


FIG. 6

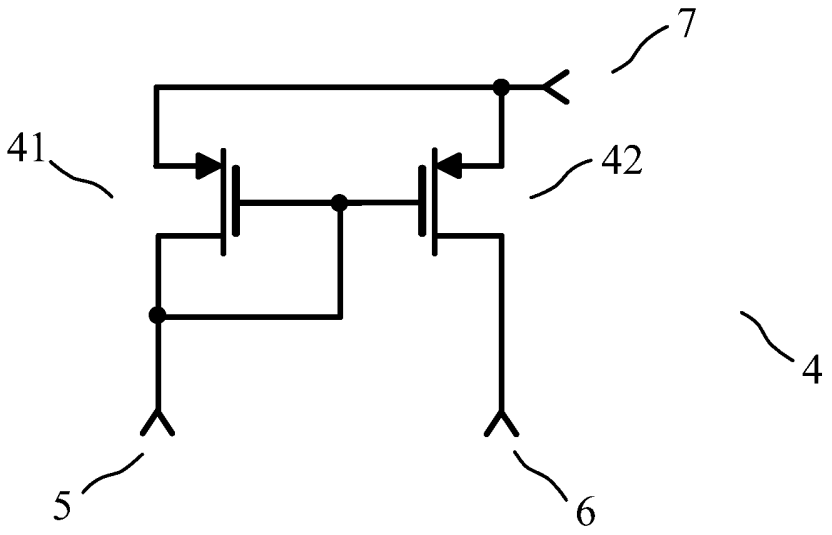


FIG. 7

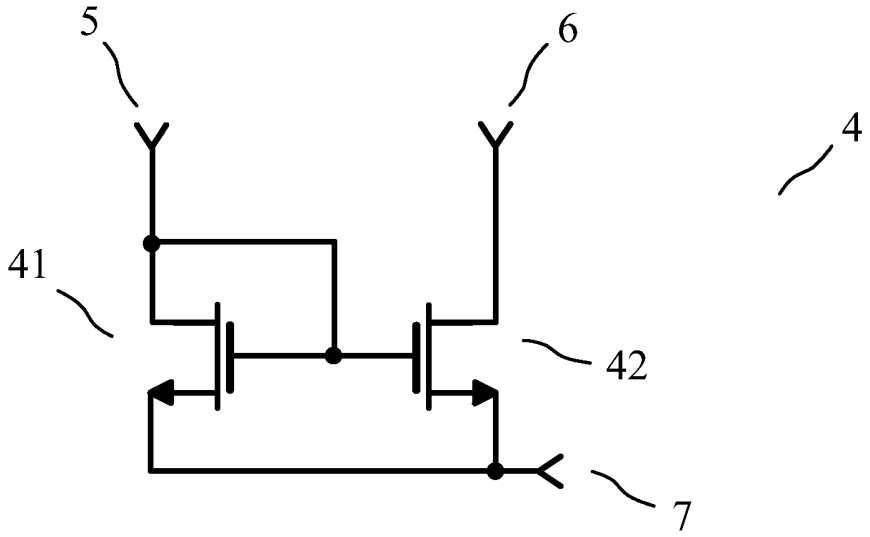
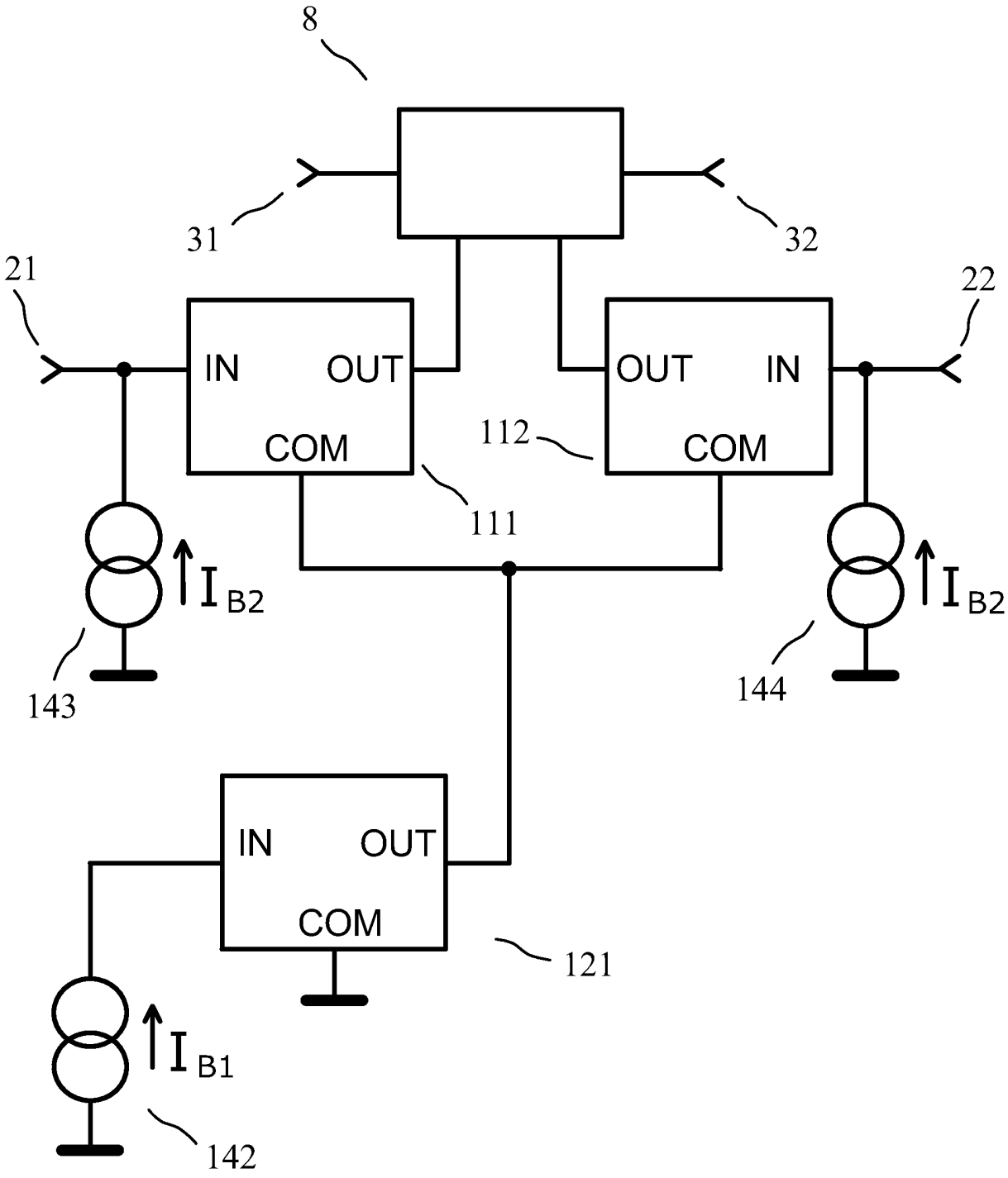


FIG. 8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I_{B1}
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FIG. 9

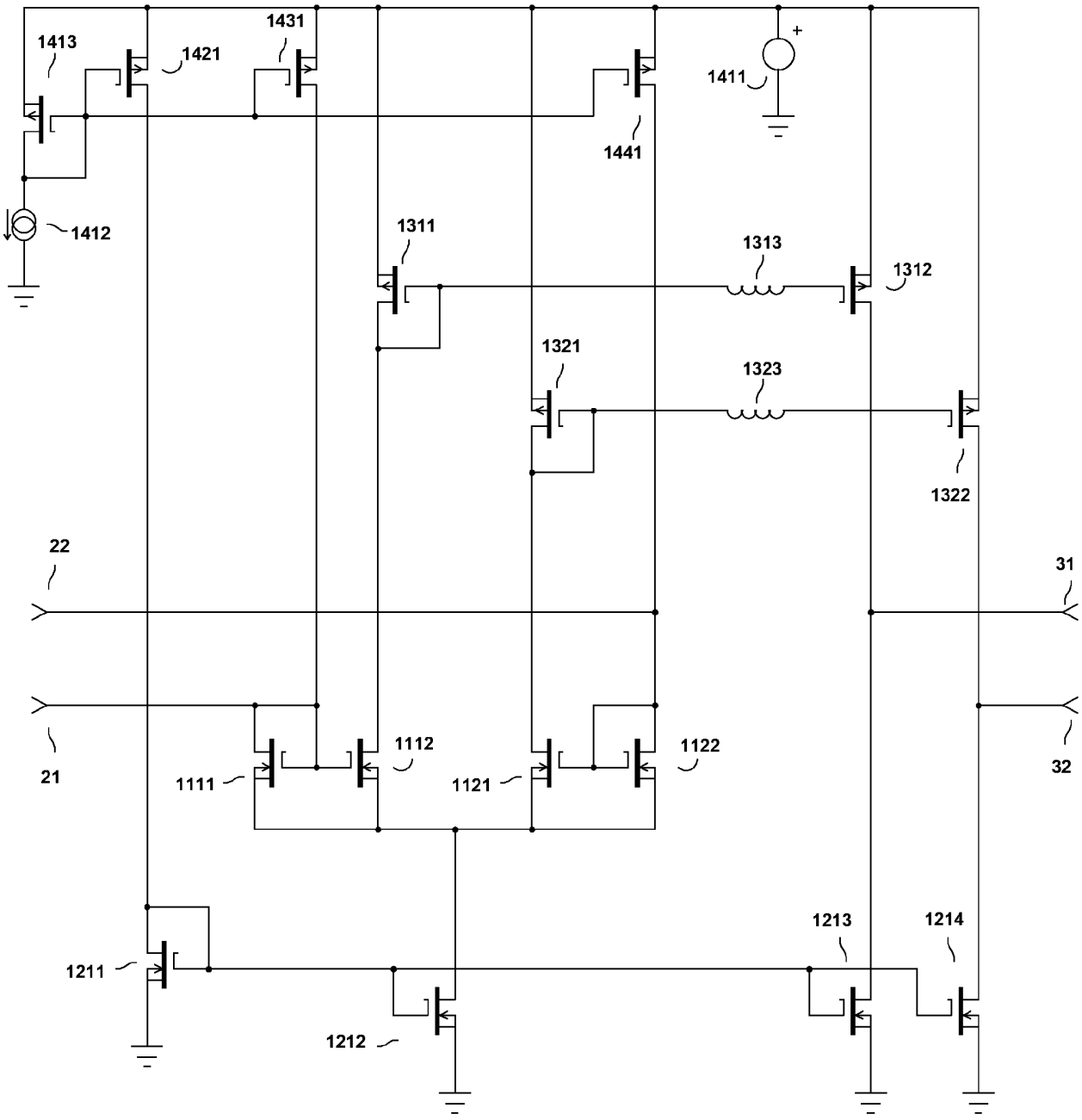
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FIG. 10

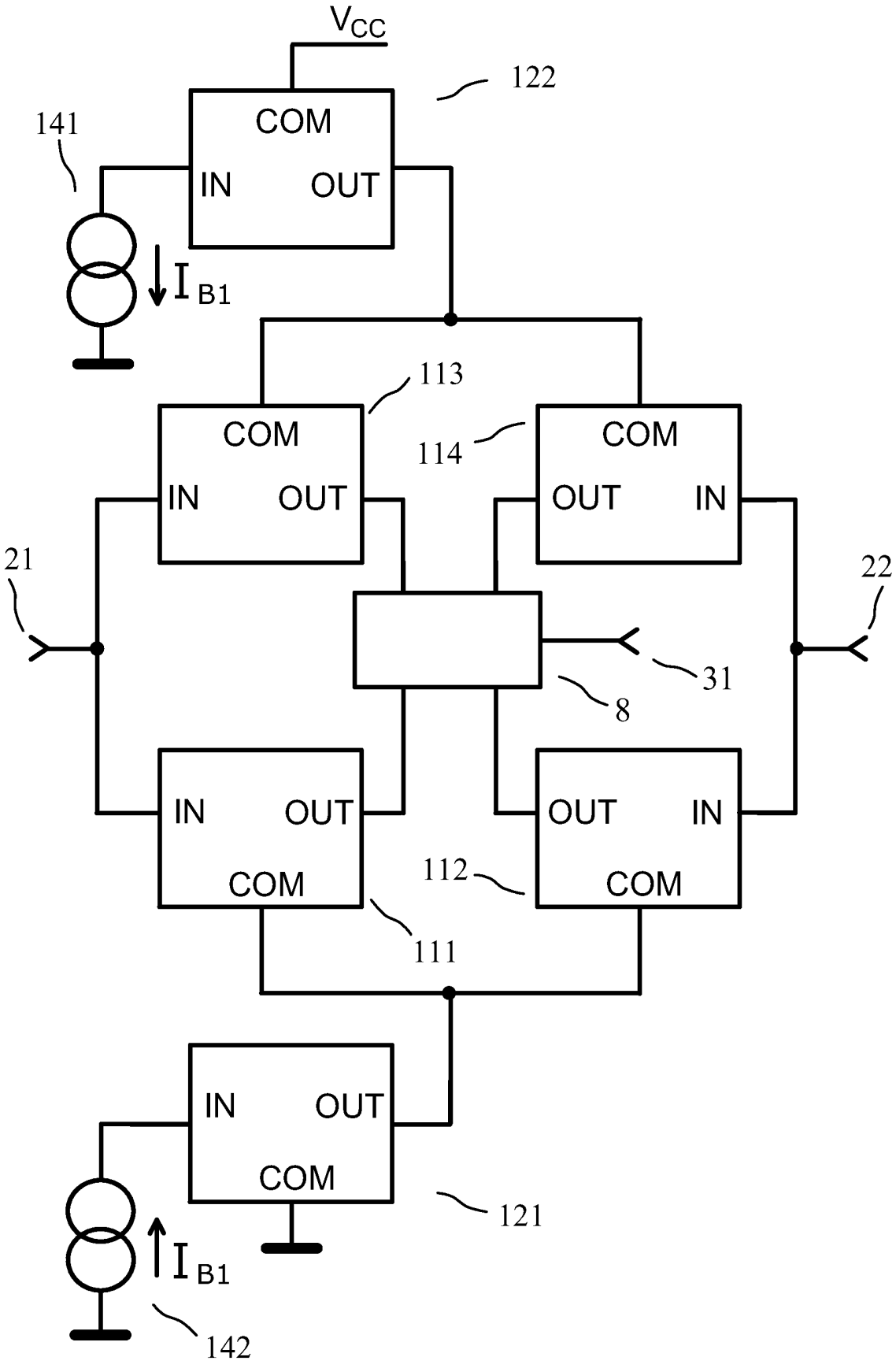
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FIG. 11

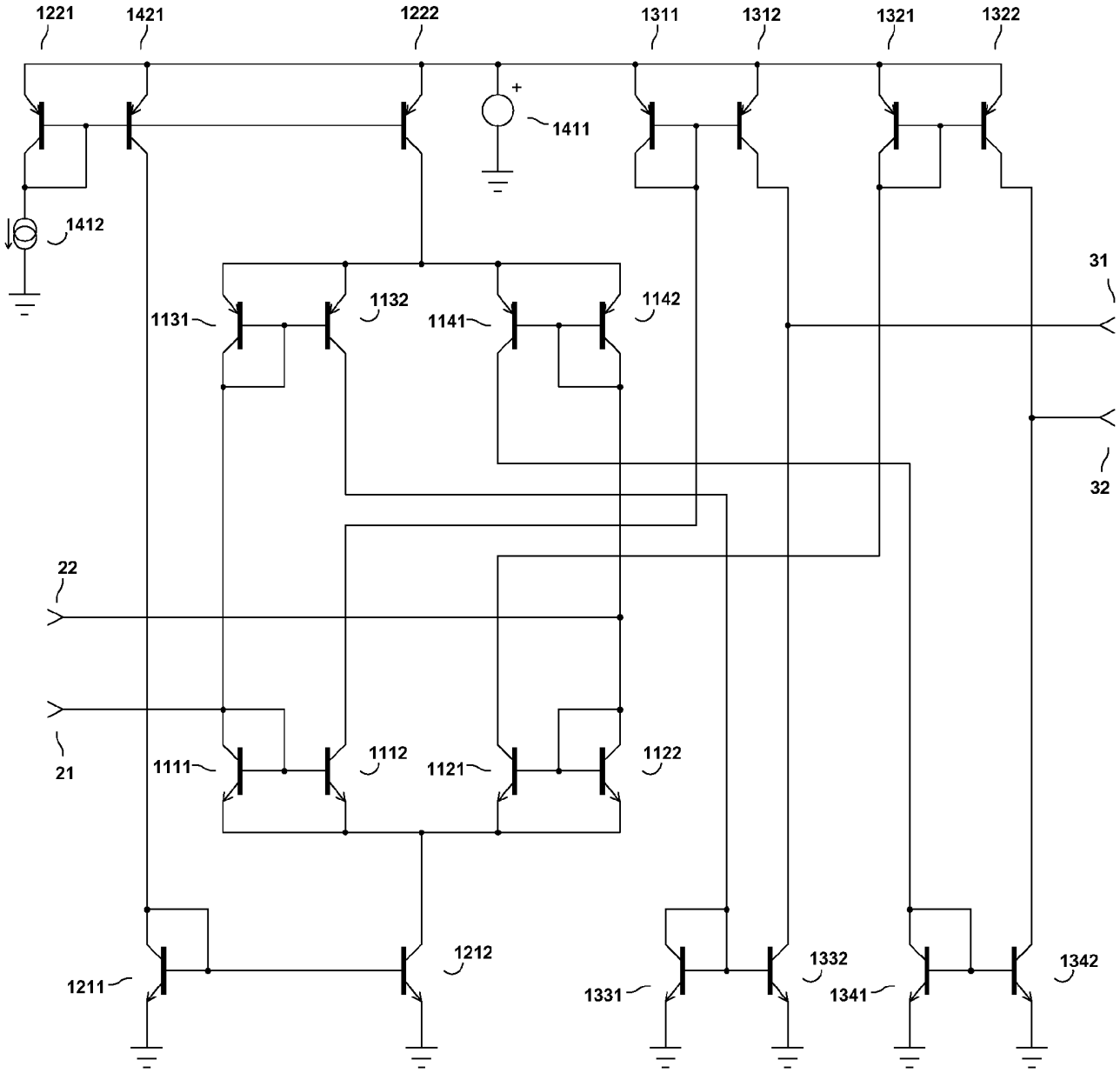
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FIG. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2011/052213

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/45
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007/099564 A1 (DIXIT ABHAY [US] ET AL DIXIT ABHAY [US] ET AL) 3 May 2007 (2007-05-03) cited in the application paragraph [0014] - paragraph [0015]; figure 2	1-10
A	US 5 483 194 A (GENEST PIERRE [FR]) 9 January 1996 (1996-01-09) column 5, line 13 - column 7, line 33; figure 2	1-10
A	US 5 132 640 A (TANAKA TATSUO [JP] ET AL) 21 July 1992 (1992-07-21) column 4, line 16 - column 5, line 33; figure 3	1-10

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 September 2011	20/09/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Lorenzo, Carlos

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2011/052213

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 5 986 501 A (RAFATI HAMID [US] ET AL) 16 November 1999 (1999-11-16) column 5, line 35 - column 7, line 49; figure 3b -----	1-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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